NCR 761
CASSETTE TERMINAL RECORDER

CONTENTS

761 CASSETTE TERMINAL RECORDER

OBJECTIVES:

Describe the NCR 761.

Give function and location of all electrical components.

Define interconnecting lines.

Explain operational sequence using flow charts.

Give circuit description of power supply.

INTRODUCTION

The NCR 761 Cassette Terminal Recorder (CTR) is a freestanding device capable of reading or writing on a tape cassette cartridge. The 761 can be used with the following systems: NCR 270 and 280 series terminals, NCR 775 Bank Proof Encoding Machines, NCR 250 Electronic Cash Register, or any new system using a Terminal Control Unit (TCU). The cassette terminal recorder performs encoding, decoding, error checking, and recording control functions. The 761 can operate as a permanent or portable unit, depending on the type of connector cable used. The model number variations are illustrated in figure 1.

The NCR 761 Cassette Terminal Recorder is also available as a portable unit. It is connected to the TCU by a single cable with a quick disconnect connector which plugs into the front of the unit. This method of connection permits the unit to be moved easily from parent unit to parent unit to load programs and send or receive data.

MODEL NUMBER: NCR 761-01-01/x/x/xx

APPLICATION

Standard	1
Bank proof	2
Portable	3

VOLTAGE

85-110 vac	1
103-127 vac	2
115-140 vac	3
180-210 vac	4
200-240 vac	5
220-260 vac	6

LANGUAGE

Domestic	1
Dutch	2
Italian	3
Norwegian	4
French	5
Spanish	6
Swedish	7
German	8
Danish	9
Japanese	10

Fig. 1 Model number variations table

761 CHARACTERISTICS

A data block is recorded on the tape in the following sequence: inter-record gap (IRG), preamble, data, cyclic redundancy character (CRC), postamble, and IRG. See figure 2. A filemark is a software indicator and can be used to separate different program or data contained on the same tape. A filemark block consists of preamble bits (10101010) followed by 16 zeros and postamble bits (10101010).

The IRG is an area of tape recorded with a steady positive voltage (no changes recorded). The IRG varies from 0.7 to 19.7 inches and is required between each record block. The first IRG passing the beginning of tape hole (BOT) is 1.3 inches long. All other IRG's, except those following a filemark (software indicator), are 0.8 inch long. Those following a filemark are 2.5 inches long. The postamble and preamble consist of alternate 1 and 0 bits (10101010) which are eight bits long. The number of 8-bit characters in the data portion of the tape can vary from 2 to 256 with the least significant bit recorded first. The CRC is a 16-bit character used to check for bit dropout or pickup in data only.

The recording density of the 761 is 800 bpi or 100 characters per inch. The bit transfer rate is 6,000 bits per second at a forward speed of 7.5 inches per second. The BOT and EOT markers are located approximately 18 inches from either end of the recordable portion of the magnetic tape.

ENVIRONMENT SPECIFICATIONS

Environment	Minimum	Maximum
Temperature	50°F	100°F
Relative humidity (max. wet bulb temp of 79°F without condensation)	20%	80%
Altitude	Sea level	12,000 ft.
Storage temp.	-40°F	+160°F
Storage humidity	5%	95%

Fig. 3 Environment specifications table

POWER SUPPLY CONNECTIONS (STRAPPING)

The power supply operates on single phase ac voltage input with a range of 85 to 260 vac at 50 or 60 Hz. One transformer is used for both input frequencies. The input can vary from 47 to 63 Hz. without affecting the output.

The following table (Fig. 4) illustrates the input and output connections of the M32-1-761 power supply. Included are the strapping options for the various input ac voltages which can be accommodated.

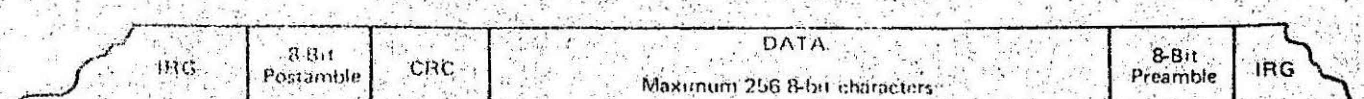


Fig. 2 Data block tape format

INPUT VOLTAGE RANGE VAC	CONNECTION	JUMPERS
85-110	TB1 3 TO TB3 2	TB3 1 TO TB3 5 & TB3 2 TO TB3 6
100-130	TB1 3 TO TB3 3	TB3 1 TO TB3 5 & TB3 3 TO TB3 7
115-140	TB1 3 TO TB3 4	TB3 1 TO TB3 5 & TB3 4 TO TB3 8
180-210	TB1 3 TO TB3 6	TB3 2 TO TB3 5
200-240	TB1 3 TO TB3 7	TB3 3 TO TB3 5
220-260	TB1 3 TO TB3 8	TB3 3 TO TB3 5

Fig. 4 Power supply strapping table

STRAPPING SIDE A OR B OF CASSETTE

The 761 can be programmed so that the transport can read side A or B of a cassette or side A only. The standard mode of operation is using the cassette on side A or B which requires a jumper wire (JPR1) to be soldered between E3 and E1 on the M64-1-761 TTL circuit board. The side A option can be field-modified for operation on side A by removing the E1 end of the jumper and connecting it to E2.

DIMENSIONS

11 inches deep

14 inches wide

6 inches high

WEIGHT

20 pounds

CONNECTION TO PARENT UNIT

For cabling instructions and proper ac connections, refer to the parent machine manual.

J14 is 280 connecting point.

761 COMPONENTS

The 761 is made up of several different modules: M64-1-761 cassette terminal adapter, M63-2-STD magnetic tape cassette transport, M32-1-761 power supply, M24-1-STD cable assemblies, and M30-1-761 miscellaneous module.

Modules referred to in this manual are called by their common names. The M64-1-761 Cassette Terminal Adapter is referred to as the CTA. The M63-2-STD Magnetic Tape Cassette Transport is referred to as the transport. The M32-1-761 Power Supply is referred to as the power supply. The M30-1-761 miscellaneous module is composed of all other parts that make up the 761. When any part of the M30 is referred to, it is called by its common name, such as cabinet, lid, etc.

CTA (M64-1-761)

The CTA is the interface between the TCU and the transport. The CTA decodes the function requested by the TCU and activates the lines to the transport to accomplish that function. The CTA consists of two printed circuit board cards. One of the cards contains TTL logic components, and the other card contains MOS logic.

The CTA controls encoding, decoding, error checking, and recording control functions. Data is recorded in 8-bit characters serially, 100 characters to the inch, with the least significant bit recorded first. The CTA checks data read or written by the transport for bit pickup or dropout by the generation of a cyclic redundancy check (CRC). The CTA generates status characters which are sent to the TCU. These status characters indicate to the TCU the condition of the CTA and the transport.

TRANSPORT (M63-2-STD)

The transport moves the cassette magnetic tape as instructed by the CTA. The transport can move the tape forward or reverse at slow speed, rewind the tape at high speed, read data from tape, write data to tape, erase a block of data from the tape, sense the presence or absence of a cassette, and determine if side A or B of the tape is up. The transport is able to determine if dark tape, clear leader, or BOT/EOT hole is positioned over the sensor. The transport is not able to determine which clear portion of the tape is over the sensor, only that the tape is clear or dark. The transport is not able to perform any operation without some outside source to direct it, such as the CTA.

Cassette Terminal Adaptor

POWER SUPPLY (M32-1-761) (See page 22)

The power supply provides most of the operating voltages required by the 761 (+12v., -12v., and +5v.). All three output voltages are internally regulated. The power supply can operate with an external ac voltage range of 85 vac to 260 vac. The different voltage ranges are compensated for by strapping options on the input of the power supply.

The M64-1-761 MOS circuit board receives its power (+12 vdc, -12 vdc, and -6.8 vdc) through the common port from the parent machine. The +12 volts is also used in the TTL circuit board. The remainder of the 761 receives power from the M32-1-761 power supply.

CONNECTOR CABLES (M24-1-STD), (M24-1-761), (M24-3-761)

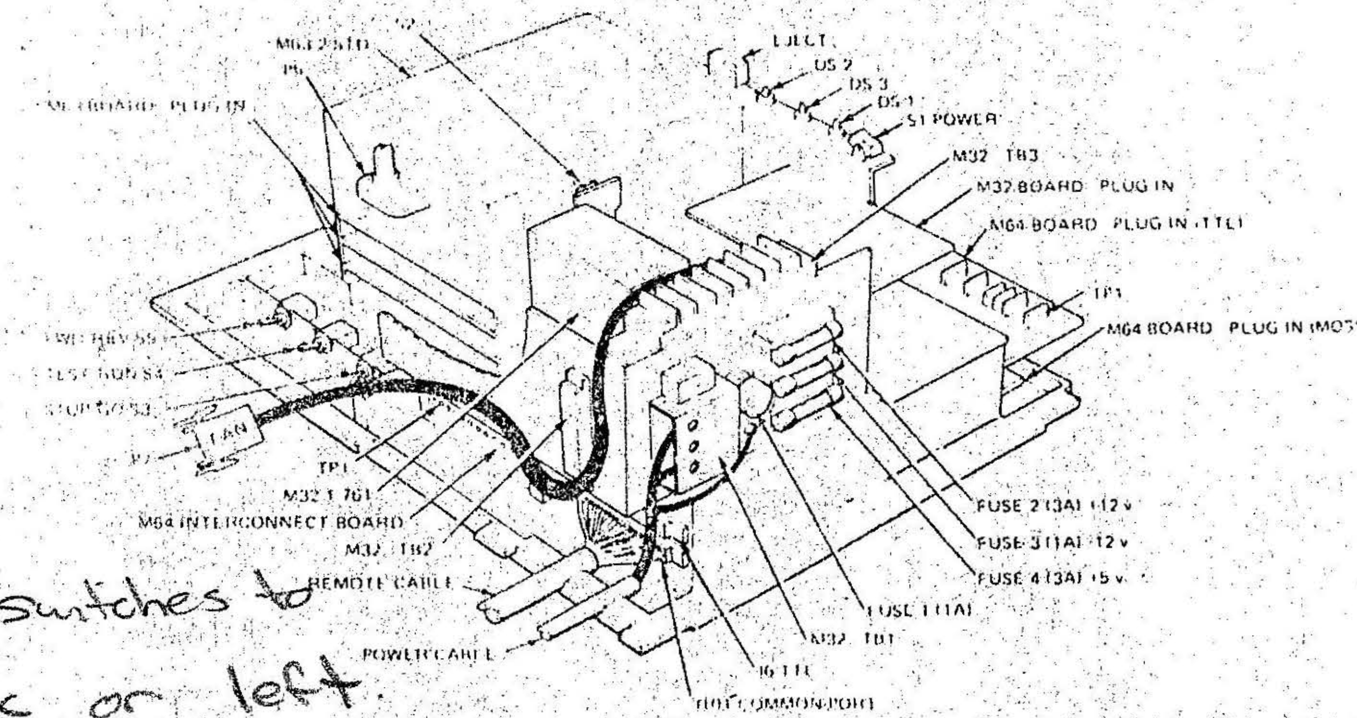
The 761 is connected to a TCU by a single cable made available in three different configurations. A standard connector cable (M24-1-STD) is permanently attached to the 761 unit and is used on permanent installations. The Technical Representative must disconnect the plug in order to change the unit to another parent machine.

A portable connector cable (M24-1-761) which plugs into the front of the 761 unit is also available. This cable is identical to the standard cable except that it has a plastic cover over the circuit board driver. The portable connector cable allows the operator to move the 761 unit from parent machine to parent machine.

Another connector cable (M24-3-761) is available for use with the 775. It has a portable quick disconnect connector and carries all the power and data lines between the 761 and the TCU. This method of connection permits the unit to be moved easily from parent unit to parent unit to load programs and send or receive data.

MISCELLANEOUS (M30-1-761)

The miscellaneous module is comprised of all other components not identified as CTA, transport, or power supply. The 761 is contained in a cabinet 11 inches deep by 14 inches wide by 6 inches high which is part of this miscellaneous module.



all switches to back or left. For Normal Opp.

Fig. 5 Cassette terminal recorder

OPERATIONAL DESCRIPTION

OPERATOR CONTROLS

There are two operator controls and three operation signal lights on the NCR 761. The controls and lights are located on the top front area of the cassette handler under the lid cover (Fig. 5).

The power switch controls the ac power to the M32-1-761 power supply. When the ac power is present, the ON light illuminates.

The Eject button causes the cassette cartridge to eject in a raised position so that it can be removed easily from the cassette transport. The cassette tape should be rewound to the clear leader before it is removed.

The B-side indicator illuminates when the B side of the cassette is in position for read or write. The 761 units can be programmed so that cassette side A/B or side A only can be used. If the 761 is programmed to use side A only, use of side B causes the 761 to be inoperative. In this case, an INOP status is issued from the CTA.

The Recording indicator illuminates when opaque tape is detected by the transport. The indicator is extinguished when there is clear leader over the cassette opening and the transport is stopped. When the light is out, the operator is informed that the cassette can be removed.

SERVICE CONTROLS

Three service switches* are located inside the cabinet and to the back of the 761 unit (Fig. 5) for use by the Technical Service Representative while servicing the unit.

Switch S3 GO/STOP controls the motion of the tape. S3 is a momentary switch and, when moved to the GO position the cassette tape starts movement.

The TEST/RUN switch (S4) is normally placed in the RUN position and can select either test or run mode. When in the TEST position, the FWD/REV switch is active only if the remote cable or MOS board of the M64 is unplugged. It is then possible to run the tape forward or reverse with the FWD/REV switch. The TEST position bypasses the lid switch which enables the operation of the 761 with the cover off for servicing.

Switch S5 FWD/REV is used to initiate forward or reverse motion of the tape.

TTL LOGIC SYMBOLS

LOGIC LEVELS

Logic levels can be explained in terms of True and False or High and Low. Since True and False levels can be whatever the designer wishes them to be, this explanation is stated in terms of High and Low positive logic levels.

In logic applications, it should be noted that some packs are used in two logical forms. For instance, the NAND gate can be used to perform an AND or an OR function. Also, some gates can be used with active Low outputs or inputs in one application and active High inputs or outputs in another application. See figure 6.

WIRED AND WIRED OR

Packs that have an open collector output can perform a wired OR or a wired AND function. The output is paralleled with the outputs of other open collector packs and connected to the proper load resistor to ensure correct logic voltages. The proper load resistor ensures that the output voltage to all connected inputs and parallel outputs

* Old style

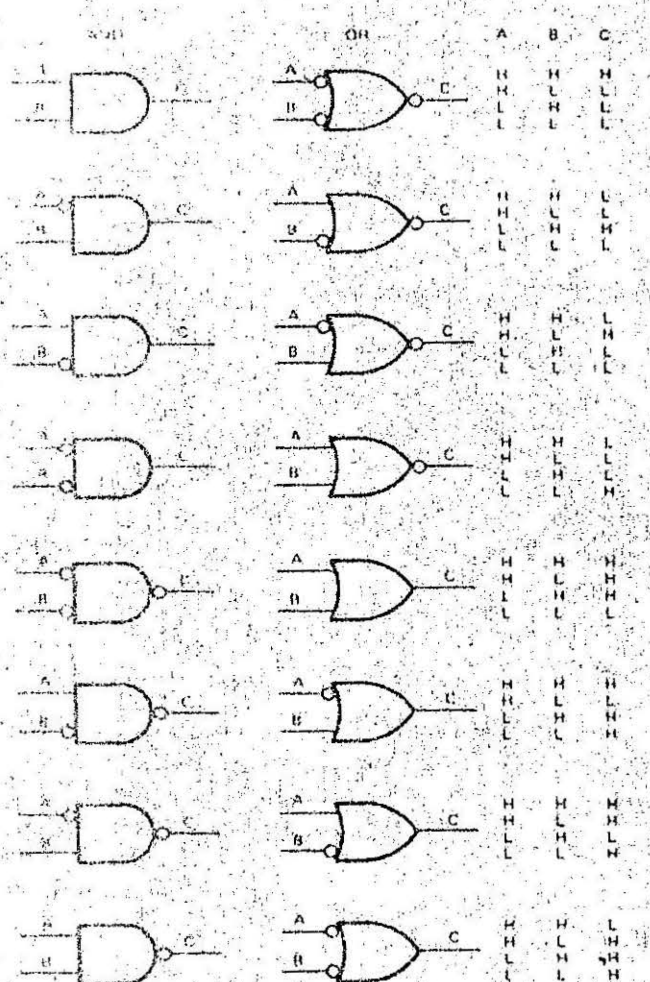


Fig. 6 Dual logic functions

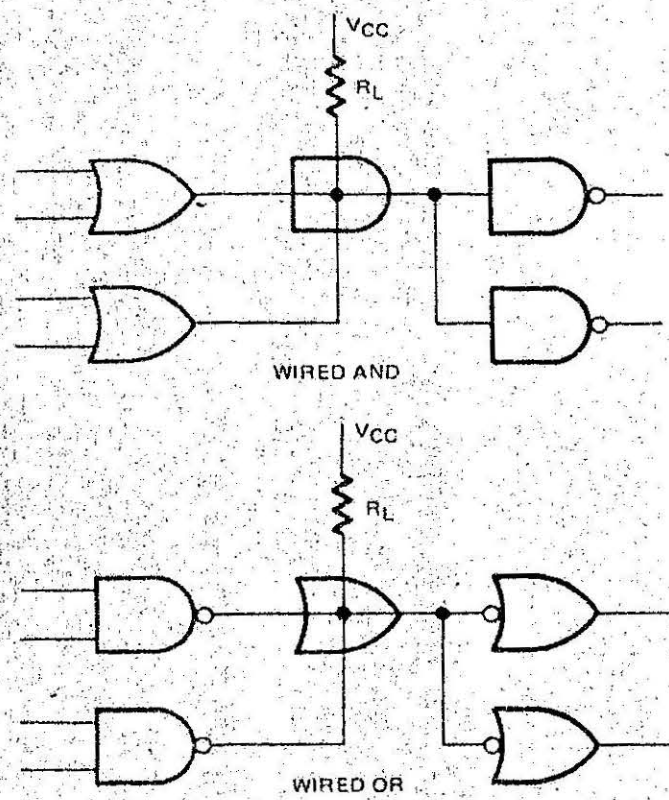


Fig. 7 Wires AND, wired OR

does not go below the logical High level if none of the paralled outputs are Low. The proper load resistor also ensures that the output voltage does not rise above the logical Low level when one or more of the paralleled outputs are Low. It should also be noted that most of the unused inputs are either connected to other used inputs or to +5 v. These connections are made so that maximum operating speeds can be obtained. However, some inputs are left open (no connection) when speed is not a critical factor. In cases where inputs are left open, they are usually shown on the logic schematics for troubleshooting purposes. See figure 7.

STATE INDICATOR

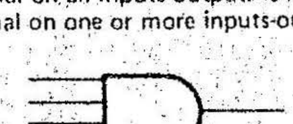
In general, the presence or absence of a small circle at the input(s) and/or output(s) of a logic symbol indicates the voltage level which activates a logic function. The small circle is not a negation symbol. The presence of a small circle at the input or output of a logic symbol indicates the function is active when it is in the Low state (0 v.). The absence of the small circle indicates that the input or output is active in the High state (+5v.).

BASIC LOGIC SYMBOLS

Positive logic levels used in this explanation are +5 v. High, 0 v. Low. See figure 8.

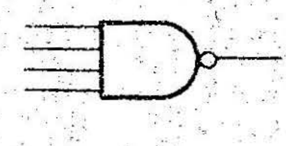
AND

High signal on all inputs-outputs is High.
Low signal on one or more inputs-outputs is Low.



NAND

High signal on all inputs-output is Low.
Low signal on any or all inputs-output is High.



OR

High signal on any input-output is High.
Low signal on all inputs-output is Low.

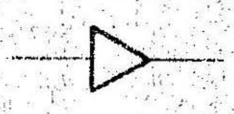
Fig. 8 Logic symbols (1 of 2)

EXCLUSIVE OR

High and Low signal combination of inputs-output is High.
High signal on both inputs-output is Low.
Low signal on both inputs-output is Low.

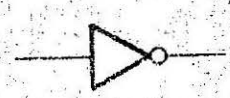
AMPLIFIER

High signal in-High output.
Low signal in-Low output.



INVERTER

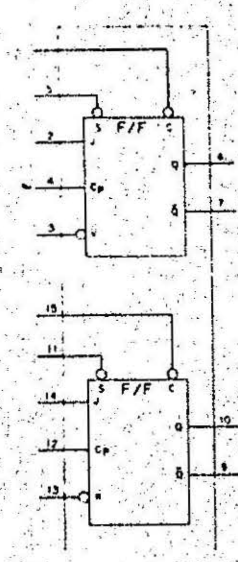
High signal in-Low output.
Low signal in-High output.



NOR

High signal on either or both inputs-output Low.
Low signal on both inputs-output is High.

Fig. 8 Logic symbols (2 of 2)



FUNCTION TABLE							
DIRECT OPERATION				CLOCKED OPERATION			
INPUTS		OUTPUTS		INPUTS BEFORE CLOCK		OUTPUTS AFTER CLOCK	
S	C	Q	Q/	J	K	Q	Q/
L	L	H	H	L	L	L	H
L	H	H	L	L	H	Q_0 (No change)	$\bar{Q}_0$
H	L	L	H	H	L	$\bar{Q}_0$ (Toggle)	Q_0
H	H	SYNCHRONOUS INPUTS CONTROL		H	H	H	L

C Direct Clear Input
Cp Clock Pulse Input
H High Voltage Level
J Clocked Input
K Clocked Input
L Low Voltage Level
Q Output
Q/ Output
S Direct Set Input
Pin 8 Ground
Pin 16 +5V
Typical Delay 22 nsec
Toggle Frequency 25 MHz

Fig. 9 Dual JK flip-flop

DUAL JK FLIP-FLOP

This chip contains two flip-flops, both of which can be set and reset by either a direct or clocked operation. An example of a Dual JK f-f is illustrated in figure 9. Direct operation overrides the clocked operation and occurs when one or both of the set (S) or clear (C) inputs are Low. When both the S and C inputs are High, clocked operation is permitted.

In some cases, the S and C inputs are used and the clocked inputs J, K, and CP are not used. Frequently, all the inputs are used so the respective flip-flop may be set and reset by both a direct and clocked operation.

During direct operation, the respective S and C active Low inputs set and reset the flip-flops. Normally, when S is Low, the flip-flop sets; when C is Low, it resets. If both S and C are Low, both outputs are High. If both S and C are High, the outputs may not change state unless a clocked operation occurs.

During clocked operation, the next state of the flip-flop is determined by the state of J and K prior to the Low to High transition of clock at CP. If J and K are both Low when clock rises, the flip-flop resets. If J and K are both High, the flip-flop sets. When J and K are in their active states, J is High and K is Low. The flip-flop toggles on the rise of clock. When J and K are in their inactive states, J is Low and K is High. The flip-flop does not change state on the rise of clock.

DUAL MONOSTABLE MULTIVIBRATOR

This chip contains two one-shots which are both retriggerable by input transitions and resettable by an active Low level input at CD. The duration of their output pulse is a function of the external resistor and capacitor timing components RX and CX. Each time the input conditions for triggering are met, the external capacitor is discharged; and a new cycle is started.

Successive inputs with a duration shorter than the output pulse retrigger either one-shot and result in a continuous High at Q, pin 6 or 10, and Low at Q/, pin 7 or 9. Retriggering is inhibited by tying the Q/ output at pin 7 or 9 back to the active Low level trigger input.

Triggering is independent of transition times and occurs on the rising edge of an input signal at the active High input if T5 or T11 is High or if T4 or T12 is Low. Each one-shot outputs a continuous High at Q and a Low at Q/ when T5 or T11 is Low or T4 or T12 is High. A Low level signal applied to the CD input, pin 3 or 13, resets the one-shot to make the Q output at pin 6 or 10 Low and Q/ output at pin 7 or 9 High. Refer to figure 10.

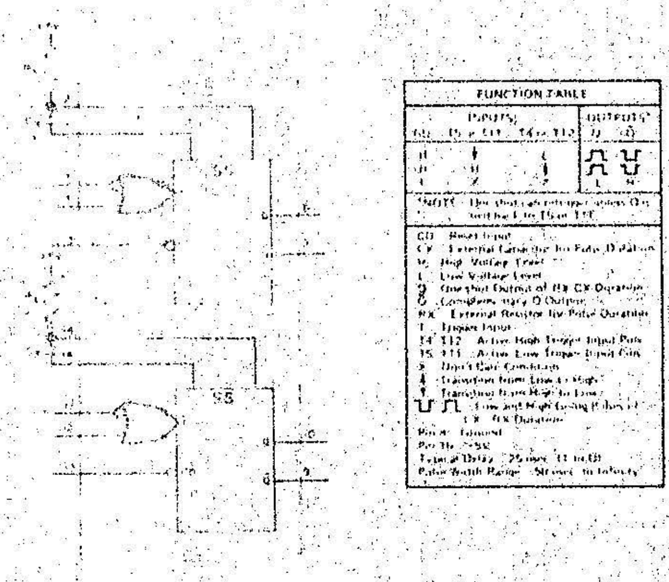


Fig. 10 Dual monostable multivibrator

FUNCTIONAL DESCRIPTION

OVERALL INTERCONNECTION (TCU-CTA-TRANSPORT)

The relationship of all the modules and circuit boards is given in figure 11. Major logic terms and pin numbers are shown along with some of the terminal and circuit boards. It should be noted that the interconnection plug board between the MOS and the TTL logic board contains test points TP-1 through TP-15.

INPUT/OUTPUT LINES.

Output Lines From CTA to TCU, UDS.3A/.

Data and status characters are transferred serially from the CTA to the common port over a common line. The data is transferred with low-order bit first. Unit status is continuously output except when a data character is transferred. The status code contains 4 bits and is in bit positions 5 through 8 of the character. A change in status must occur between bit 5 and bit 8.

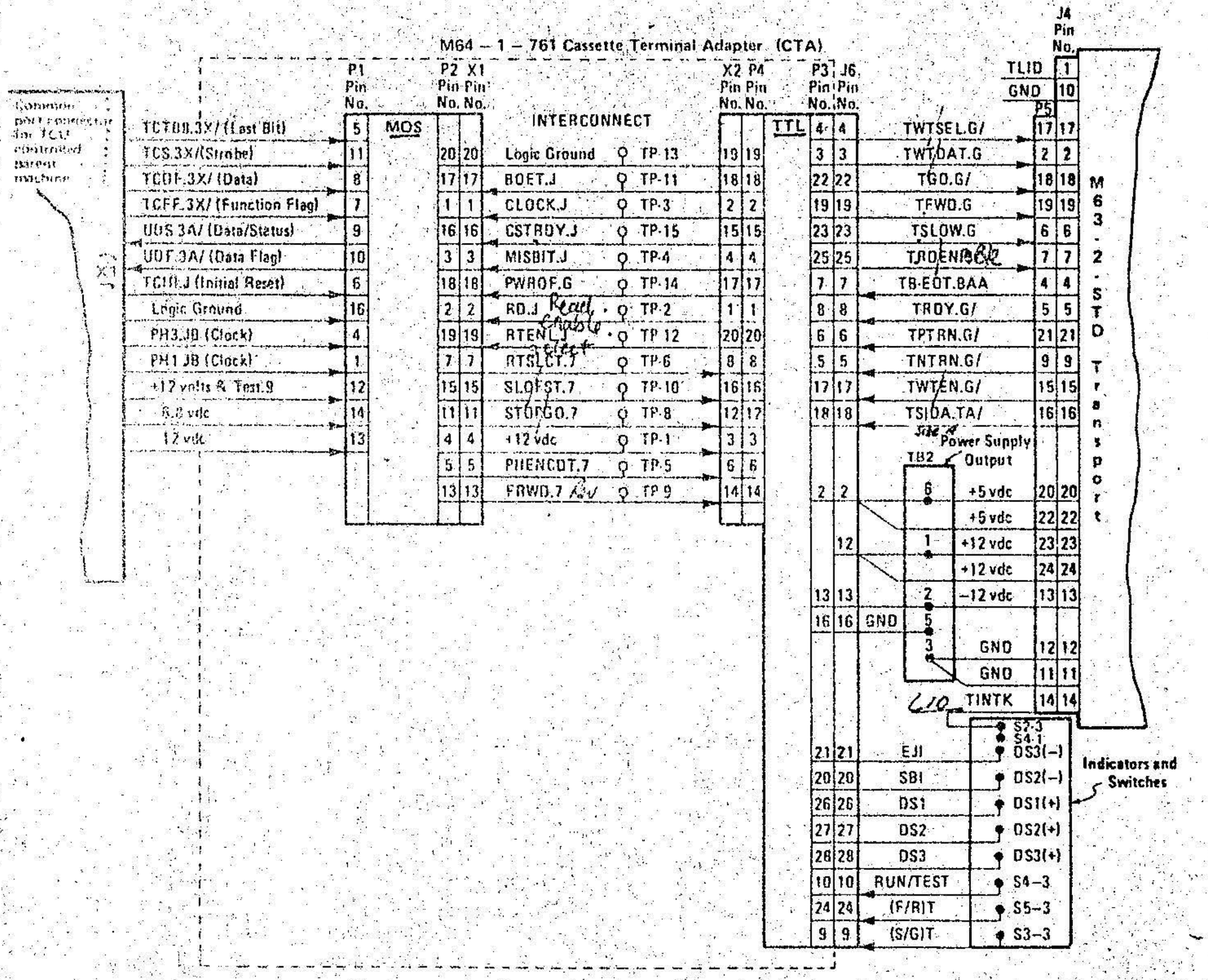


Fig. 11 Overall interconnection

UDF.3A/

The data flag identifies the information transferred on the UDS line as data or status. When a data character is transferred, the data flag is High for one character time. When a status character is transferred, the data flag is Low.

Input Lines From TCU to CTA
TCDF.3X/

Data and function characters are transferred from the common port to the CTA over a common line. Data and function characters contain 8 bits each and are transmitted with low order bit first. The first 4 bits (b1-b4) of the function character are ignored by the CTA logic. The last 4 bits (b5-b8) are the function code which identifies the function to be performed by the CTA logic.

TCFF.3X/

The function flag identifies the information transferred on the TCDF line as data or function. When a function character is transferred, the function flag is High for one character time. When a data character is transferred, the function flag is Low.

TCS.3X/

The strobe frames the data or function character on the data/function (TCDF.3X/) line and signals the CTA logic which is connected to the port (specified by the port address field of the instruction) to accept the character on the line.

TCTB8.3X/

TCTB8 is a 1 bit timing pulse which is High during the last bit time of an 8-bit character. It identifies the high-order bit of the character (bit 8).

PH1.JB and PH3.JB

The TCU clock provides phases 1 and 3 of the 4-phase clock to the CTA-MOS logic circuit board.

TCIR.1

TCIR initializes the CTA logic on powerup. It also inhibits operation of the CTA and the M63-2-STD transport whenever the voltage levels common to the TCU and CTA vary from the specified limitations if the phase 4 clocks are inoperable or if manual control of the TCIR is exercised. A High on the TCIR line inhibits system operation.

+12 vdc

The +12 vdc is supplied to the CTA MOS and TTL circuit board from the port of the TCU.

-6.3 vdc

This voltage is supplied to the MOS circuit board from the port of the TCU.

-12 vdc

This voltage is supplied to the MOS circuit board from the port of the TCU.

Lines Between The TTL and MOS Board
RTSLCT.7

The RTSLCT.7 (write select) line from the MOS board is level converted in the TTL circuit board to TWTSEL.G/ for output to the transport. When RTSLCT.7 is High, the write mode of operation is active. When RTSLCT.7 is Low, the write head in the tape transport is inhibited. The desired state of the write select line is established in coincidence with or prior to the initiation of tape motion by means of the STOPGO.7 line.

PHENCDT.7

The PHENCDT.7 (write data) line from the MOS board is level converted to TWTDAT.G for output to the transport. The write data line provides the serialized phase encoded information from the CTA to be recorded by the transport.

STOPGO.7

The STOPGO.7 (stop/go) line from the MOS board is level converted to TGO.G/ for output to the transport. A High level on the STOPGO.7 line causes tape motion. Tape direction and speed are determined by the forward/reverse (FRWD.7) and slow/fast (SLOFST.7) lines. This line changes to a High level after the forward/reverse and slow/fast lines reach their steady states. STOPGO.7 is Low to stop tape motion before the forward/reverse and slow/fast lines change state.

FRWD.7

The FRWD.7 (forward/reverse) line from the MOS board is level converted to TFWD.G for output to the transport. This line determines tape direction. A Low level on this line (FRWD.7) causes forward motion, and a High level causes reverse motion.

BOET.J

The BOT/EOT line from the transport is converted to BOET.J for output to the MOS board. BOET.J is Low whenever the BOT/EOT marker or clear leader is positioned over the photoelectric sensor in the transport.

RTENL.J

The TWTEN.G/ (write enable) line from the transport is double inverted to RTENL.J for output to the MOS board. RTENL.J is Low whenever a write enable plug is sensed on a cassette.

CLOCK.J

This term is input to the MOS board from the TTL board. A clock pulse is generated for each bit of data.

CSTRDY.J

This term inhibits the motion of the transport for 250 msec. after the end of rewind or when the cassette is loaded or the cassette door is closed on the transport. This delay allows the head assembly in the transport sufficient time to pull in.

MISBIT.J

This term indicates to the MOS circuitry that a missing bit was detected during read or write.

PWROF.G

When this term is High, it indicates that the +5 vdc supply is off or has failed. Normally, when this term is High it indicates that the cassette is not powered up.

RD.J

This line supplies the data read from the transport to the MOS.

SLOFST.7

The MOS circuit board controls this logic term. When SLOFST.7 is Low, the transport operates at a slow speed.

Output Lines From CTA to Transport
TWTDAT.G

The write data input line provides the serialized phase encoded information from the CTA to the M63-2-STD transport.

TFWD.G

The forward/reverse line determines tape direction. A High level on this line causes forward tape motion, and a Low level causes reverse tape motion.

TSLOW.G

A High level on this line causes the tape to move at a slow speed. A Low level causes tape to move at fast speed.

TGO.G/

A Low level on this stop/go line causes tape motion. Tape direction and speed are determined by the forward/reverse and slow/fast lines. This line changes to a Low level after the forward/reverse and slow/fast lines reach their steady states. The stop/go line goes High to stop tape motion before the forward/reverse and slow/fast lines change states.

TWTSEL.G/

When the write select line (TWTSEL.G/) is Low, the write mode of operation is active. When the write select line is High, the write head in the tape transport is inhibited. The desired state of the write select line is established in coincidence with or prior to the initiation of tape motion by means of the stop/go (TGO.G/) line.

TRDEN.G/

When the read enable line (TRDEN.G/) goes Low, it conditions the transport electronics to permit data on the read data (TPTRN.G/ and TNTRN.G/) lines. A High on the line (TRDEN.G/) inhibits data flow from the transport.

Input Lines From Transport to CTA
TPTRN.G/

The read data line provides a digital signal for a postive transition of the recorded phase encoded data from the transport. A positive transition represents a 1 bit if the transition falls within clock time.

TNTRN.G/

The read data line provides a digital signal for a negative transition of the recorded phase encoded data from the transport. A negative transition represents a 0 bit if the transition falls within clock time.

TB-EOT.BAA

This line is held High whenever the BOT/EOT marker or clear leader is positioned over the photoelectric sensor in the transport.

TRDY.G/

The ready line (TRDY.G/) is High whenever the tape is not loaded or the cassette door is open.

TWEN.G/

The write enable line is Low to enable the write circuits when a write enable plug is sensed on a cassette.

TSIDA.TA/

This line is Low when recording on side A of the cassette and High for side B.

CONTROL CODES

The TCU is the controlling unit in all 761 operations. See figure 11 for the relationship among the TCU, CTA, and transport modules. The TCU has eight function codes that can be sent to the CTA (fig. 12) to initiate the various 761 operations. The CTA has nine status codes that can be sent to the TCU (fig. 13) to indicate the condition of the 761. The function and status codes are explained in more detail in the following text.

Function	Code Bits 8 7 6 5
Stop (STOP)	0 0 0 1
Write (WRT)	0 0 1 0
Read (RED)	0 0 1 1
Backspace (BSP)	0 1 0 0
Rewind (RWD)	0 1 0 1
Erase (ERS)	0 1 1 0
Move (MOV)	0 1 1 1
Write filemark (WTFM)	1 0 0 1

Fig. 12 Function codes table

Status	Code Bits 8 7 6 5
Busy (BSY)	0 0 0 1
Inoperative (INOP)	0 0 1 0
Power off (PWOF)	0 0 1 1
Idle (IDL)	0 1 0 0
BOT/EOT (BET)	0 1 0 1
Filemark (FLMK)	0 1 1 0
Error (ERR)	0 1 1 1
Ready (RDY)	1 0 0 0
End of message (EOM)	1 0 0 1

Fig. 13 Status codes table

STATUS CODE DESCRIPTION

The following status codes are issued from the CTA to the TCU.

Busy (BSY)

The busy status indicates that the CTA is performing a previously assigned task or that the data buffers are not ready to send or receive data.

Inoperative (INOP)

The inoperative status is issued when the transport is not ready and the 761 power supply is turned ON.

Power Off (PWOF)

The power off status is issued when the 761 power supply is turned OFF.

Idle (IDL)

The idle status is issued when the CTA is ready for another function.

BOT/EOT (BET)

The BOT/EOT status is issued when the CTA has detected a BOT or EOT hole or clear leader during the previous operation.

Filemark (FLMK)

The filemark status is issued when the CTA has detected a file mark during a read operation.

ERROR (ERR)

The error status indicates that data was read or written incorrectly. An error occurs if tape movement is greater than 2.8 sec. (19.7 inches) without data detection or clear leader is sensed for greater than 3.0 sec. (22 inches) during write, read, backspace, or erase.

Ready (RDY)

The ready status is either a request for more data from the TCU to the CTA when in the write mode or a request to move data from the CTA to the TCU when in the read mode.

End of Message (EOM)

The end of message status indicates the end of a data message or tape movement greater than 19.7 inches or 2.8 sec. without data detection during a read operation. It also indicates the detection of an inter-record gap (IRG) during a backspace or erase operation.

FUNCTION CODE DESCRIPTION

The following function codes are issued from the TCU to the CTA.

Stop (STOP)

The stop function is issued at the end of a message during a write operation or to terminate a read, backspace, erase, or rewind operation.

Write (WRT)

The write function is issued when data is to be written on the cassette.

Read (RED)

The read function is issued when data is to be read from the cassette.

Backspace (BSP)

The backspace function is issued when the cassette is to be backspaced over one block of data.

Rewind (RWD)

The rewind function is issued when the cassette is to be rewound to the beginning of tape or clear leader.

Erase (ERS)

The erase function is issued when one block of data is to be erased from the cassette. The erase function erases tape in the reverse direction. This function is the same as backspace except that the write select line is turned on for erase. See flowchart in figure 16 for backspace.

Move (MOV)

The move function is issued when the data is to be transferred from the CTA to the TCU.

Write filemark (WTFM)

The write filemark function is issued when a filemark is to be written on the cassette.

FUNCTION CODE FLOWCHARTS

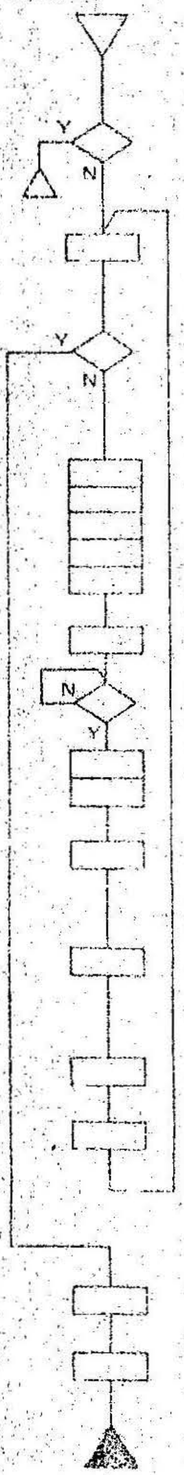
The function codes are used by the TCU to initiate the various operations of the 761. The following flowcharts illustrate a general operational sequence of the operations initiated by the function codes. The flowcharts do not go into the detail of the circuit board logic; however, the charts do indicate major logic terms that pass from one board to another. The intent of the flowcharts is to provide the Technical Representative with a general understanding of the 761 operations, not necessarily used for troubleshooting.

It should be noted that during the read, write, backspace, and erase operations, the 2.8 sec. timer checks for data on the tape. When no data is present for 2.8 sec. or 19.7 inches, the tape is stopped. It is necessary for the TCU to issue another function code in order to continue that same operation. For instance, it is necessary to issue many erase (ERS) function codes in order to erase a complete tape if the tape contains very little data. If the tape is full of data, the complete tape could be erased with only one ERS function code.

The flowcharts illustrated in figures 14 through 19 represent an operation with one function issued. The TCU determines the sequence, the proper function code, and the number of times the function codes are used.

Rewind Tape to Clear Leader

A rewind function code (fig. 14) can be used to rewind a cassette tape. It is necessary to use a backspace function preceding the rewind in case the tape is already on clear leader. When the tape is on clear leader, the CTA does not know if the tape is at the beginning or end. Using the backspace function first, establishes the position of the tape.

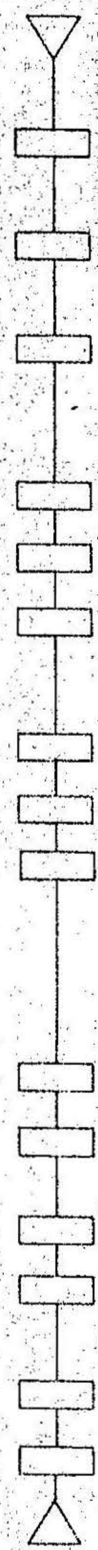


		Rewind function issued to rewind tape to beginning of tape (clear leader).
	BET	Does BET status exist? If yes, then a backspace function is necessary preceding rewind.
	RWD	Rewind function issued to CTA (CTA ready - power on, tape loaded, and lid closed).
	ERR	Error status issued to TCU? Error status indicates clear leader only, which indicates the tape is rewound.
	TGO	Start tape.
	TSLOW	Fast speed.
	TFWD	Rewind (reverse direction).
	TWTSEL	Do not write.
	TRDEN	Disable read.
	BSY	Busy status issued to TCU.
	TB EOT	BOT/EOT or clear tape?
	TGO	Stop tape.
	TSLOW	Slow speed.
	Delay	255 msec. delay (stop time and delay for head assembly in the transport to pull in).
	BET	Issue BET status to TCU. This indicates clear leader or EOT/BOT.
	STOP	Issue stop function to CTA.
	BET or IDL	CTA issues idle status if BOT is detected. BET status is issued if tape is on clear leader (It may be necessary to initiate another rewind function if not on clear leader).
	STOP	Stop function issued to CTA.
	BET	Issue BET status to TCU. CTA is in the IDL mode at this time.
	End	

Fig. 14 Rewind function

Clear Leader to Past BOT Marker

After a new cassette is installed or after a rewind operation, clear leader should be under the read/write heads. In order to position the tape 2.8 sec. past the BOT hole, a read or write function is necessary. The flowchart in figure 15 illustrates the correct positioning of the tape when a read function is issued to the CTA. If a write function is issued, the operation is the same except that tape erase is in effect to clear the tape.

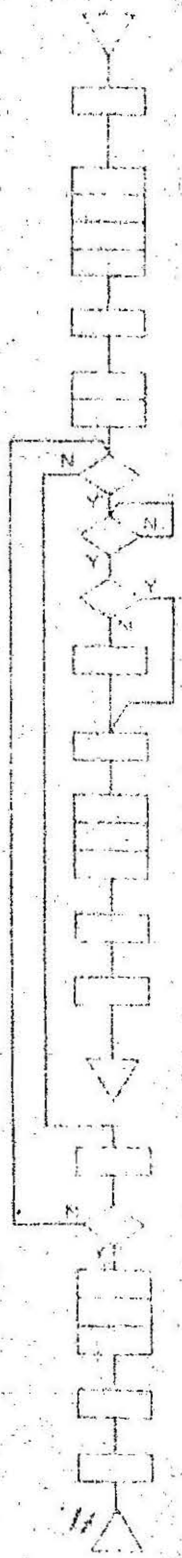


		Move tape from clear leader to past BOT marker in read mode. (Start read or write positions)
	BET	BET status issued to TCU indicating BOT/EOT or clear leader from previous operation.
	RED	Read functions issued to CTA (CTA ready - power on, tape loaded, and lid closed).
	TGO TSLOW TFWD TWTSEL TRDEN	Start tape, slow speed, forward direction, do not write, do not read.
	BSY	Busy status issued to TCU.
	TB-EOT	Lose clear leader.
	Delay	Start 2.8 sec. delay to monitor presence of data. If data is detected then an erroneous condition exists.
	BOT/EOT	Tape moves past BOT marker.
	TRDEN	Read data from tape 30 msec. after detecting BOT.
	DATA	If data is detected during the 2.8 sec. time out, ready status is indicated by the CTA. The 2.8 sec. timer is reset and the tape stops at the next IRG. Then the BOT/EOT status is checked to ensure that the tape has moved past the BOT.
	Delay	End 2.8 sec. delay.
	TGO TFWD TRDEN	Stop tape, disable tape forward, and disable read.
	Delay	25 msec. stop time.
	BET	Issue BET status to TCU. If BET status is not present then an erroneous condition exists.
	STOP	Stop function issued to CTA.
	IDL	CTA goes into idle mode.
	End	Tape is positioned 2.8 sec. past BOT for read or write operation.

Fig. 15 Mode tape from clear leader to past BOT marker

Backspace

The backspace function (fig. 16) drives the tape in the reverse direction to the next EOT, BOT, clear leader, or IRG, whichever occurs first. If the CTA senses clear leader for greater than 3.0 sec. or data is not detected from the tape for 2.8 sec., the CTA goes into the error mode and issues ERR status. If data is sensed before 2.8 sec., the CTA continues in the backspace mode until an IRG is sensed and the CTA issues an EOM (end of message).

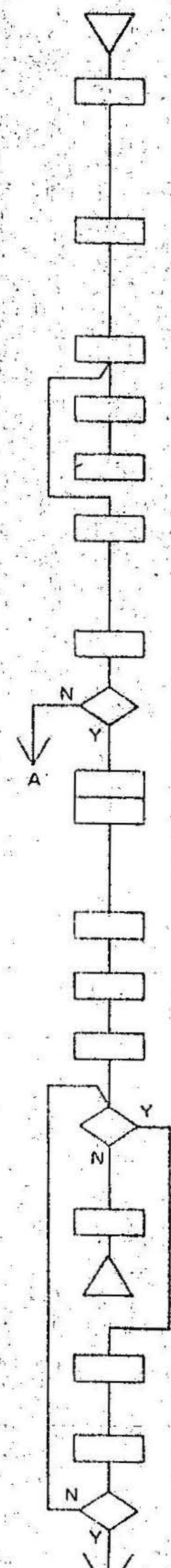


		Backspace
BSP		Backspace function issued to CTA.
TGO		Start tape.
TSLOW		Slow speed.
$\overline{\text{TFWD}}$		Tape reverse.
Delay		Start 30 msec. timer.
BSY		Issue busy status to TCU.
Delay		End 30 msec. delay.
$\overline{\text{TRDEN}}$		Read data from tape.
DATA		Data detected?
IRG		IRG detected?
BOT/EOT		BOT/EOT detected?
EOM		End of message status issued to TCU.
Delay		20 msec.
$\overline{\text{TGO}}$		Stop tape.
TRDEN		Disable read.
BSY		Issue busy status to TCU.
Delay		25 msec. stop time.
IDL or BET		CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End		
Delay		2.8 sec.
Delay		End of 2.8 sec. delay?
$\overline{\text{TGO}}$		Stop tape.
TRDEN		Disable read.
BSY		Issue busy status to TCU.
Delay		25 msec. stop time.
ERR		Error status issued to TCU.
End		

Fig. 16 Backspace

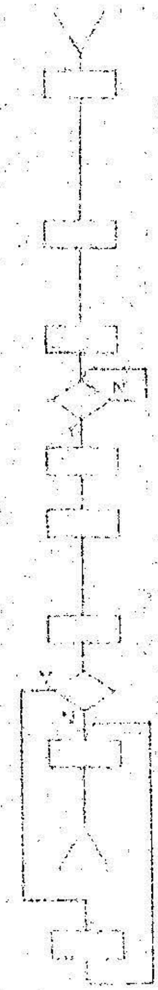
Write Data Block

The data write can start at the beginning of a new tape or at an IRG. The write data function flowchart illustrates this operation (fig. 17). Forward erase can be accomplished during the write function when data is all zeros.



	Writing Data Block (WRT).
WRT	Write function issued to CTA. Tape has previously been set to the correct position. CTA is in idle mode. Write enable plug present on cassette.
TGO TFWD $\overline{\text{TWTSEL}}$ TSLOW	Start tape, forward direction, write select, slow speed.
BSY	Busy status issued to TCU.
Delay	30 msec.
$\overline{\text{TRDEN}}$	Read data from tape.
Delay	64 msec. IRG delay (allows tape to get up to normal speed and generate the proper inter-record gap).
RDY	Ready status issued to TCU.
	Is this a write operation? If not write a filemark.
DATA-1 Preamble	First 8-bit character to be written sent from TCU to CTA. CTA developes preamble and transport starts writing preamble on tape (10101010).
BSY	Busy status issued to TCU.
RDY	Ready status issued to TCU.
DATA-1	Send data-1 from CTA to transport.
DATA	Did TCU respond with next data character within 1.1 msec. after (RDY) ready status?
ERR	Error status issued to TCU.
End	
BSY	Busy status issued to TCU. Transfer data to transport.
RDY	Ready status issued to TCU.
DATA	End of data?

Fig. 17 Write data block (1 of 2)

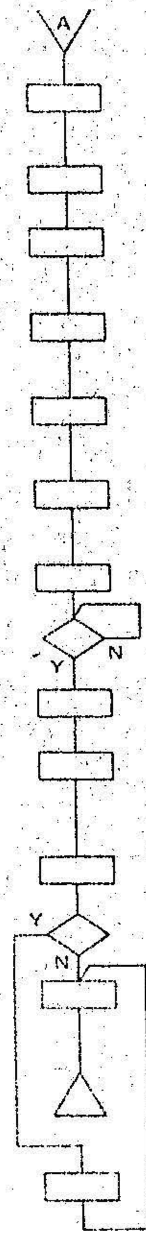


STOP	Stop function issued to CTA when the data block is complete. The stop function enables the CTA to send CRC and postamble to the transport.
CRC & Postamble	Send CRC and postamble from CTA to transport.
Read	Read after write for error check.
IRG	IRG detected?
Delay	28 msec.
TGO TFWD TRDEN	Stop tape, disable tape forward, disable read.
Delay	25 msec stop time.
ERR	Was error status issued to TCU?
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	
STOP	Stop function issued to CTA.

Fig. 17 Write data block (2 of 2)

Write Filemark

The first portion of this operation is the same as the write data start function. It should be noted that an exit in the write data flow leads into the write filemark operation. The write filemark function is illustrated in figure 18.



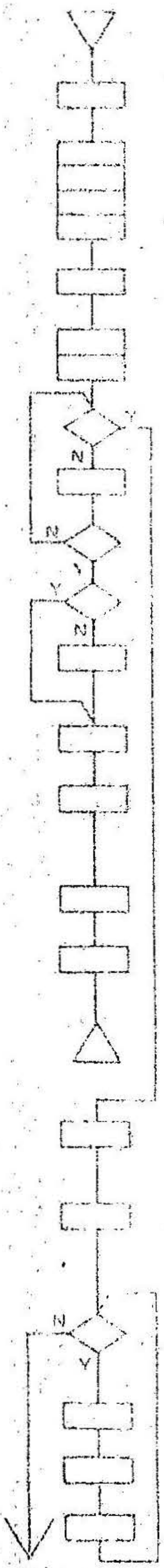
Write Filemark

WTFM	Write filemark function issued to CTA.
BSY	Busy status issued to TCU.
Preamble	Preamble sent from CTA to transport (10101010).
Filemark #1	Filemark #1 sent from CTA to transport (00000000).
Filemark #2	Filemark #2 sent from CTA to transport (00000000).
Postamble	Postamble sent from CTA to transport (10101010).
Read	Read after write for error check.
IRG	IRG detected?
Delay	28 msec.
$\overline{TGO}$ $\overline{TFWD}$ TRDEN	Stop tape, disable tape forward, disable read.
Delay	25 msec. stop time.
ERR	Error status issued to TCU?
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	
STOP	Stop function issued to CTA.

Fig. 18 Write filemark

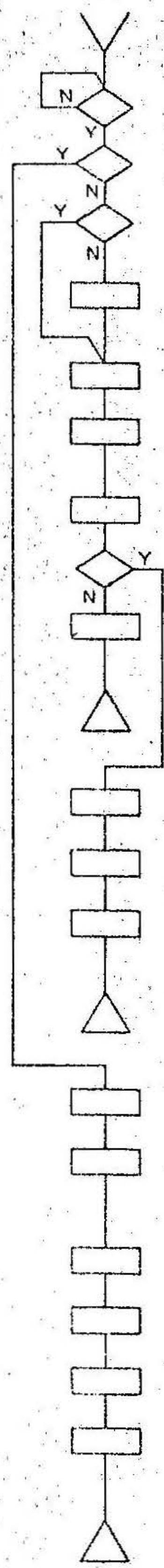
Read Data Block and Filemark

The read data function (fig. 19) can be issued at the beginning of a new tape or at an IRG. The read filemark function is included in this flowchart since it is similar to the read function.



	Reading data block & filemark.
RED	Read function issued to CTA.
TGO TSLOW TFWD Delay	Start tape. Slow speed. Forward direction. Start 30 msec. timer.
BSY	Busy status issued to TCU.
Delay TRDEN	End 30 msec. delay. Read data from tape.
DATA	Data detected?
Delay	2.8 sec.
Delay	End of 2.8 sec. delay?
EOT/BOT	EOT hole detected?
EOM	End of message status issued to TCU.
Delay	20 msec.
$\overline{TGO}$ $\overline{TFWD}$ TRDEN	Stop tape, disable tape forward, disable read.
Delay	25 msec. stop time.
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	
Preamble	Read preamble from tape into CTA.
DATA	Read 3 characters from tape into CTA (3 characters could be 1 data, 2 CRC or all 3 data characters).
DATA	Is another data character detected?
RDY	Issue ready status to TCU.
MOV	Issue move function to CTA.
BSY	Issue busy status to TCU. Transfer data to TCU.

Fig. 19 Reading data block and filemark (1 of 2)



IRG	IRG detected?
ERR	Did read error occur?
BOT/EOT	Did BOT/EOT or clear leader appear on tape?
EOM	End of message status sent to TCU.
Delay	20 msec.
$\overline{TGO}$ $\overline{TFWD}$ TRDEN	Stop tape, disable tape forward, disable read.
Delay	25 msec. stop time.
FLMK	Was this a filemark block?
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	
FLMK	Issue filemark status to TCU.
STOP	Issue stop function to CTA.
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	
Delay	20 msec.
$\overline{TGO}$ $\overline{TFWD}$ TRDEN	Stop tape, disable tape forward, disable read.
Delay	25 msec. stop time.
ERR	Error status sent to TCU.
STOP	Stop function issued to CTA.
IDL or BET	CTA changes to idle mode. If EOT/BOT hole is detected then CTA changes to BET status.
End	

Fig. 19 Reading data block and filemark (2 of 2)

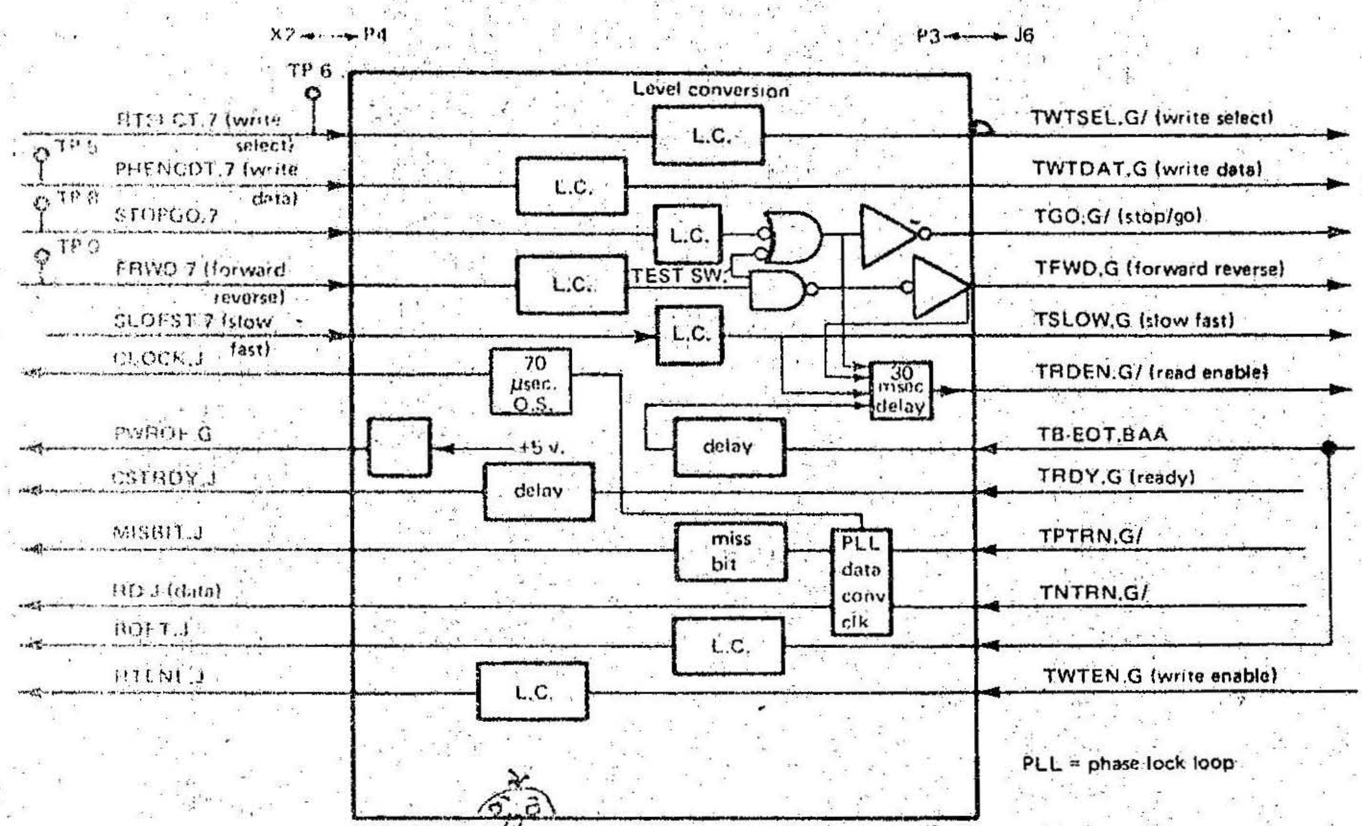


Fig. 20 TTL circuit board block diagram

Tape Erase

This function is the same as a backspace operation except that tape erase is in effect. See the backspace flowchart for similar operation (fig. 16).

CTA (CASSETTE TERMINAL ADAPTER)

The CTA is comprised of two cards working as one unit to provide the interface between the TCU and the cassette transport. One of the cards contains MOS circuitry, and the other card contains TTL discrete circuitry. The MOS card contains most of the logic functions performed by the interface. The repair philosophy of the MOS type boards is limited in the field to exchanging the bad card for a good one. Using this repair philosophy, major functions of the MOS board are explained but not the operation of individual chips or circuitry on the board. The TTL board is explained in sufficient detail so that, should repair of the board be necessary, it can be accomplished in the field.

TTL LOGIC BOARD

Most of the TTL circuit board logic functions are level conversions from MOS to TTL and TTL to MOS as illustrated in the TTL block diagram in figure 20. The other functions performed are delays, bit count of the preamble to synchronize the PLL (phase lock loop), read enable control, and clock generation. The TTL circuit board also provides cassette side selection with the programmable strapping option. The strapping option allows the use of cassette side A/B or side A only. When it is programmed to use cassette side A only, use of cassette side B causes the CTA to go into the inoperative mode and to issue an inoperative status.

Phase Lock Loop (PLL)

Data is recorded by the transport using the Manchester principle of recording. With Manchester recording, a positive-going voltage applied to the write head records a 1 bit; a negative-going voltage records a 0 bit. If two adjacent bits are the same, a phase transition (fig. 21) is used between them to give the proper voltage direction to the recorded data. As the recorded data is read, the phase transitions are blocked and not recognized as data. One function of the PLL is to screen out these phase transitions so that only data are recognized. Another area of logic that works in connection with PLL looks for a missing bit. If a 0 or 1 bit fails to appear during data transfer, MISBIT.J goes High to block any further data transmission; and the error mode is initiated.

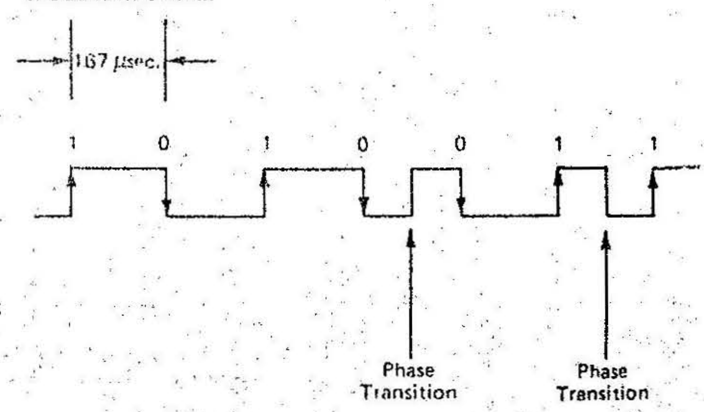


Fig. 21 Recording principle

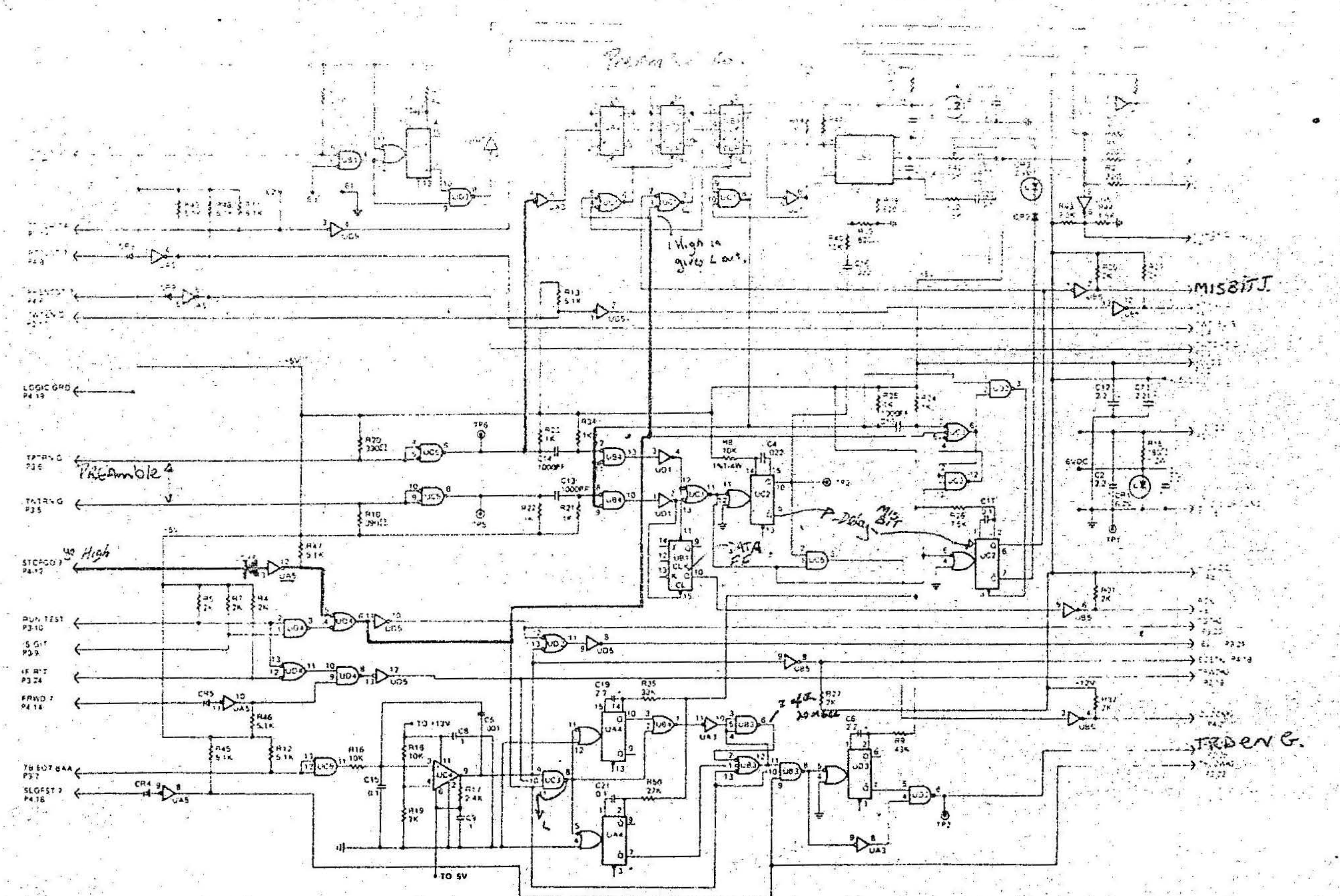


Fig. 22 TTL circuit board schematic

Data is transferred from the transport to the TTL board on the TPTRN.G7 and TNTRN.G7 lines (fig. 22). As the preamble is read, the positive transitions (1 bits) are received on the TPTRN.G7 line. The preamble is used to synchronize the phase locked loop (PLL) to the frequency of the bits received. The positive transitions are sent to a series of three f-f's. The f-f's count the preamble bits and able the gates that control the flow of data to the data f-f.

The three f-f counter counts 1 bits of the preamble and enables the PLL output on the fourth 1 bit (fig. 23). After STOPGO.7 goes High, the first positive transition sets the first f-f of the counter. The second positive transition resets the first f-f and sets the second f-f. The third positive transition sets the first f-f for the second time. The fourth positive transition resets the first f-f. The resetting of the first f-f resets the second f-f. The second f-f resetting sets the third f-f. When the third f-f sets, it blocks the first and second f-f's by holding the asynchrnous reset Low, keeping them reset.

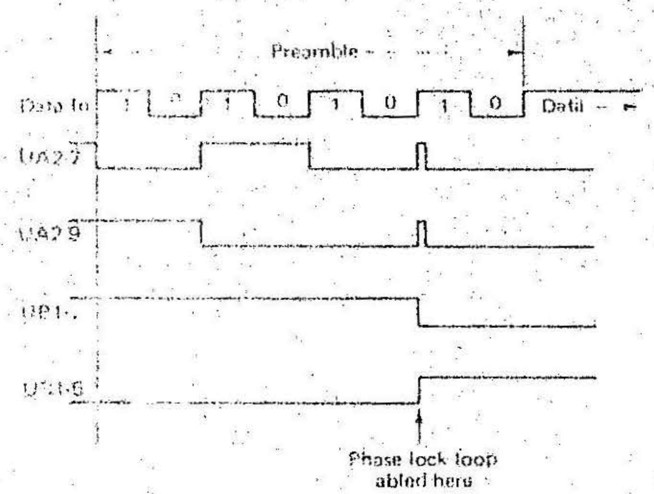


Fig. 23 Three f-f counter timing chart

The set output of the third f-f is tied to an AND gate (UC1). The other input to the AND gate is the output of the PLL (UB2). After the preamble, the output of the PLL controls the inputs to the data f-f (UB1) to block all insignificant phase transitions. When a 1 bit appears on the TPTRN line, the data f-f is set. When a 0 bit appears on the TNTRN line, the data f-f is reset.

The phase lock 70 μsec. s-s and the missed bit 220 μsec. s-s are always triggered whether the input is a 0 or 1-bit. The phase lock 70 μsec. s-s (UC2) provides control to the PLL (UB2) to blank out phase transitions in the data signal. The missed bit 220 μsec. s-s (UC2) is triggered with each data bit. The time between data bits is 167 μsec. If bits of data are present and adjacent, the missed bit s-s never times out; however, if a data bit is missed, the s-s times out, and the PLL blanks out the incoming data until the error is reset.

Read Enable

Another function of the TTL circuit board is to control the read enable line (TRDEN.G/) to the transport (fig. 23). When the read enable line goes Low, it conditions the transport electronics to permit data on the read data lines. A High on the line inhibits data flow from the transport.

Read enable is used to allow data to be read or written 30 msec. past the BOT after rewind or insertion of a new tape. Also, when starting an operation on an IRG, the read enable is delayed for 30 msec. after tape Go to allow the tape to get up to speed for read and write. The following circuit description starts after a tape has been rewound or a new one inserted.

When TB-EOT.BAA goes High, indicating clear leader (fig. 24), the output from UC4 comparator goes High after a delay of 500 to 700 μsec. This delay is provided to prevent impurities on the clear leader from being mistaken as a BOT signal. When the forward direction (FRWD.7) is selected and STOPGO.7 goes High for tape start, the output of gate UC3 goes Low, triggering UA4 20 msec. s-s and UA4 1.0 msec. s-s. The output of UB3 pin 12 latch goes High; and, with slow tape speed, the UD3 30 msec. s-s is triggered. If clear leader continues after the 20 msec. s-s times out, UB3 latch resets and read enable is disabled (TRDEN.G/ remains High). When clear leader runs out, the UB3 latch being reset prevents triggering the 30 msec. s-s. The read enable term TRDEN.G/ has remainded High. As the tape continues to move, the BOT hole triggers the 20 msec. and 1.0 msec. s-s again; and the same sequence occurs. This time, when the 30 msec. s-s times out, both pins 4 and 5 of UD2 are High, allowing TRDEN.G/ to go Low. Latch UB3 remains latched, allowing pin 4 of UD2 to remain High, since the BOT marker has since passed.

MOS LOGIC BOARD

The MOS board decodes the function codes sent from the TCU (fig. 25). Motion control terms FRWD.7, SLOFST.7, and RTSLCT.7 are also generated in this portion of MOS pack U6 for control of the transport.

A portion of pack U4 on the MOS board contains two timers. One timer is 2.8 sec. and the other is 3.0 sec. If the CTA senses clear leader for greater than 3.0 sec. or if data is not detected from the cassette for 2.8 sec. during a write, read, backspace, or erase function, the CTA changes from write to error mode.

The MOS logic controls writing a data block on a cassette, reading a data block from a cassette, backspacing or erasing a data block, or rewinding a cassette. This is accomplished

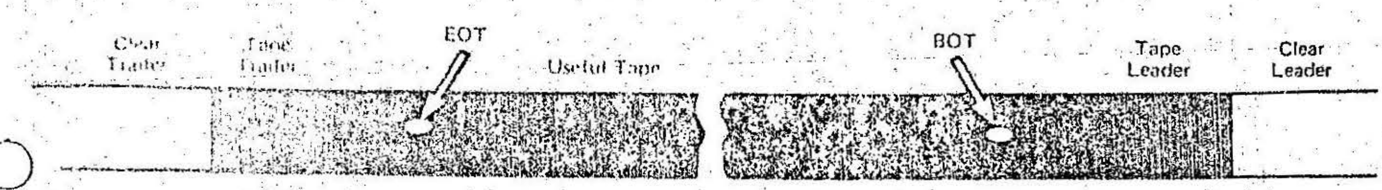


Fig. 24 Tape format

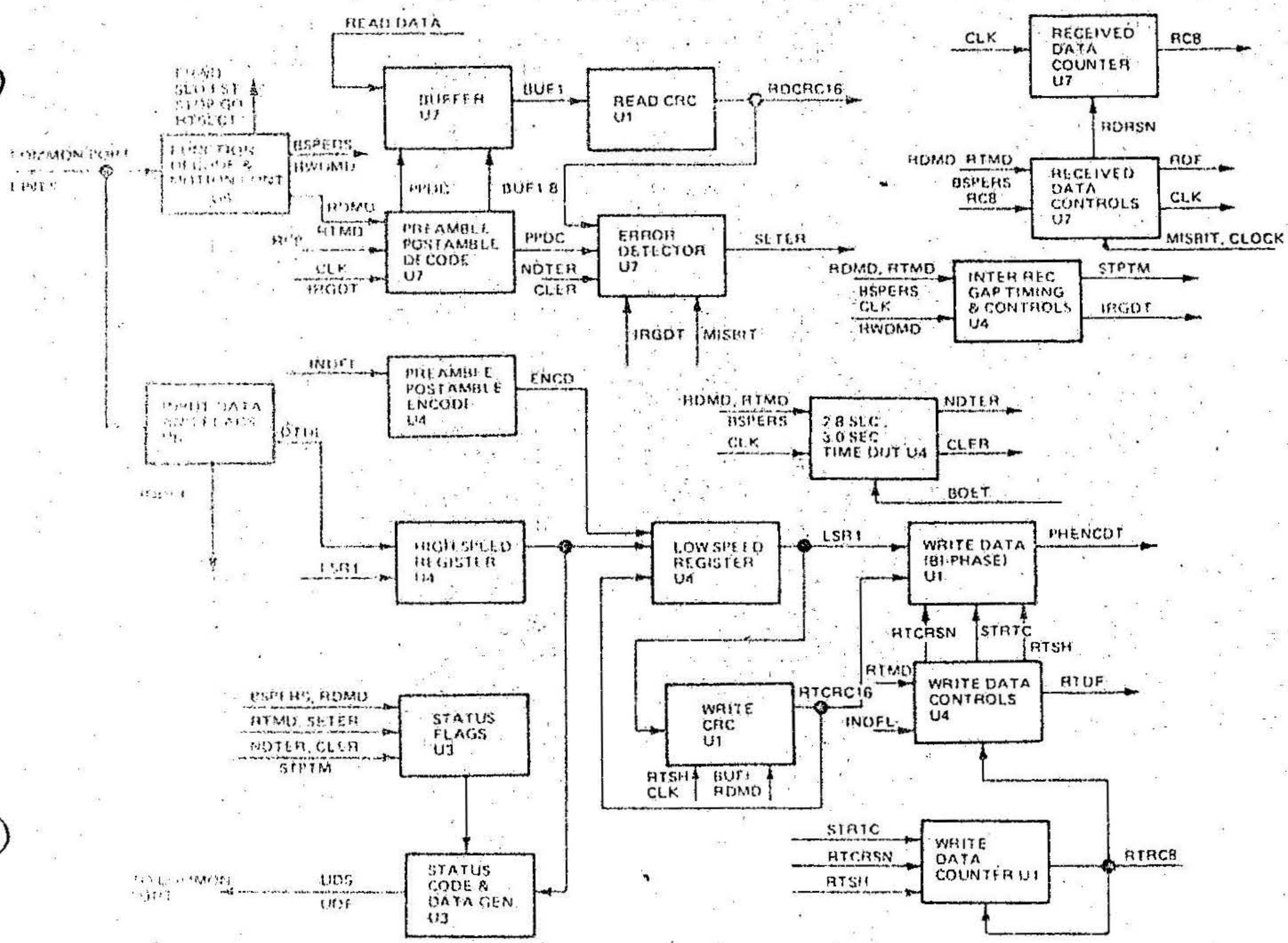


Fig. 25 MOS circuit board block diagram

by decoding the function codes sent from the TCU with MOS pack U6.

The MOS circuit board generates and transfers the preamble character immediately preceding the data block. It also generates and transfers the postamble character to the transport immediately following the CRC. MOS pack U7 decodes the preamble and postamble when reading from tape. Pack U4 encodes the preamble and postamble when writing.

The MOS board generates the cyclic redundancy character (CRC) and transfers it immediately following the data block to the transport. A portion of pack U1 handles this operation.

A portion of MOS board pack U4 generates and controls the transfer of filemark characters to the transport. The filemark consists of the preamble, 16 zeroes, and postamble.

The MOS performs the read after write operation of the recorded data on the cassette for write error detection. A portion of pack U1 reads the CRC for error detection.

MOS board pack U4 generates the inter-record gap (IRG) of approximately 0.7 inch between data records by controlling IRG timing.

During the read operation, the MOS circuit board pack U7 checks and strips off the preamble, CRC, and postamble characters from the received message before it is transferred to the TCU.

The MOS board detects system overload when receiving data. This occurs when the TCU does not take data from the CTA within a certain time. If the TCU fails to send a move (MOV) function within 1.1 msec. after the ready (RDY) status is on the port, a system overload occurs.

The CTA status codes sent to the TCU are generated in a portion of MOS pack U3. The status codes indicate to the TCU the condition of the CTA and transport.

OPERATIONAL MODES

The TCU selects the 761 by sending a predetermined port and position number. After the 761 is selected, the TCU selects the function the CTA is to perform and sends the proper function code to the CTA.

The CTA operates in one of eight modes (fig. 26). The CTA should be in the Idle mode before the TCU initiates a write, read, backspace, erase, or rewind operation. The TCU should not issue any motion function such as WRT, RED, BSP, ERS, or RWD when the CTA indicates BSY status on

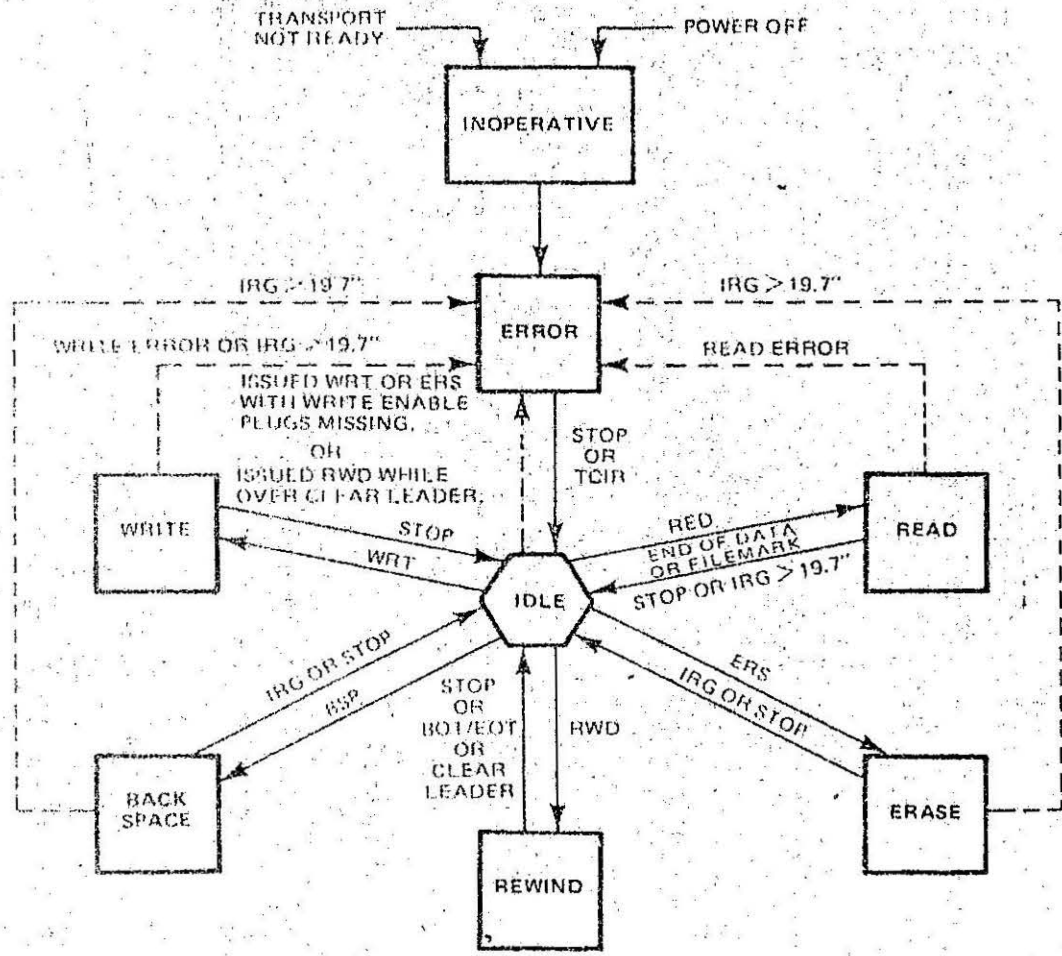


Fig. 26 Operational modes of the CTA

the port. If the CTA receives any illegal function or receives MOV or WTEM function when the CTA does not indicate a RDY status on the port, the CTA changes status to BSY without performing any operation and creates an erroneous condition.

INOPERATIVE MODE

The CTA changes into the inoperative mode, regardless of its present state, when delayed ready (CSTRDY.J) goes High or power to the transport goes off. When ready (TRDY.G) goes Low, a delay of 280 msec. is provided in order to allow sufficient time to pull in the head assembly on the transport. When in the inoperative mode, the CTA inhibits all tape movement by holding TGO.G/ High and ignores all function codes. The power off (PWOF) status is issued to the TCU when the power if OFF. The inoperative (INOP) status is issued to the TCU when delayed ready is High and power is ON. After delayed ready goes Low and the power supply is ON, the CTA goes into an error mode and changes the status to error (ERR).

ERROR MODE

When the CTA is in the error mode, it inhibits tape movement by holding TGO.G/ High and issues an ERR status 25 msec. after the stop function is issued. The CTA can be removed from the error mode only by receiving a stop function or TCIR from the TCU which puts the CTA in the idle mode and issues an IDL status within the next character time. If an error is caused by an incorrect write, read, backspace, or erase operation and a BOT/EOT marker is detected, the CTA, upon receiving a stop function, changes the ERR status to BET status.

Write or read error detection ensures correct data transfer. An error is indicated if the preamble or postamble is not correct, if data bit transitions do not occur at the correct time, and if the CRC has a character bit error. The CTA does a modulo eight count; that is, it checks to see if a non 8-bit word is read. If a problem is detected in the above checks, the CTA goes into an error mode.

The CTA goes into the error mode if any of the following occurs.

1. A write or read error is detected, and an IRG is sensed.

2. The CTA is issued a WRT or ERS function with write enable (TWTEN.G/) High.

3. System overload.

4. The system is in the inoperative mode with power ON, and delayed ready (CSTRDY.J) Low.

5. Clear leader is sensed for greater than 3.0 sec. when in the write, read, backspace, or erase mode.

6. Data is not detected for 2.8 sec. when in the backspace, erase, or write mode.

7. A rewind function is issued by the TCU when clear leader is detected by the CTA.

IDLE MODE

The initial mode of operation of the CTA is the idle mode. The CTA goes into the idle mode when the following conditions occur.

1. The CTA receives TCIR (initial reset).

2. The CTA completes a write or read operation without error.

3. The CTA detects a filemark (FLMK) during the read mode.

4. The TCU issues a STOP function. If a STOP function is issued to abort a motion operation in which an error is detected, the CTA goes into the error mode.

5. The CTA detects an IRG (inter-record gap) when in the backspace or erase mode.

6. The CTA detects a BOT/EOT marker or clear leader in the rewind mode. It is possible that the transport may or may not detect a BOT/EOT marker while in the rewind mode during high speed rewind.

When the CTA is in the idle mode, the following conditions occur.

1. Tape motion is inhibited when STOPGO.7 is Low.

2. Idle (IDL) status is issued 25 msec. after a stop function.

3. Idle (IDL) status is issued 255 msec. after a stop function if the previous operation is rewind. This delay provides sufficient time for the head assembly in the transport to pull in completely.

4. BET (BOT/EOT) status is issued in place of the IDL status if the BOT/EOT tape marker or clear leader is detected during a backspace, write, erase, rewind, or read operation.

5. BET status is changed to IDL status when the CTA receives a STOP function code and does not sense clear leader.

6. IDL status is changed to FLMK (filemark) status if a filemark is detected.

7. FLMK status is changed to BET status if a STOP function is received and the BOT/EOT marker is detected during the read operation or if clear leader is sensed.

WRITE MODE

When write enable (TWTEN.G/) goes Low, the CTA enters the write mode of operation. If TWTEN.G/ is already Low when the write (WRT) function code is issued, the CTA goes into the error mode and issues an ERR status.

Upon receiving the WRT function, the CTA puts BSY status on the port. The tape in the cassette starts moving in the forward direction caused by forward/reverse (TFWD.G) and slow/fast (TSLOW.G) going High and write select (TWTSEL.G/) and stop/go (TGO.G/) going Low. However, the CTA holds stop/go (TGO.G/) High for an additional 15 msec. if the previous tape motion was in the reverse direction. At the end of a 64-msec. delay, the tape is up to normal speed; and the IRG (inter-record gap) is established on the tape. The ready status is sent to the TCU; following this, the TCU sends to the CTA information to be written. The preamble is written first, with data next. The read after write feature generates the CRC (cyclic redundancy character) which checks for write errors. The CRC is then written on the tape, followed by the postamble. When all the data from the TCU is transferred, a stop function is issued to stop the tape. The time it takes for the tape to stop generates the IRG. The CTA goes back into the IDL mode upon completion of the write operation.

After the first data character is sent to the CTA, if the TCU fails to send a new data character or a STOP function within 1.1 msec. after the RDY status is on the port, the CTA issues BSY status and starts generation of an IRG. When the IRG is sensed by the CTA, it goes into the error mode and issues ERR status.

The CTA contains a data timer which monitors the presence of clear leader or data from the cassette during the write mode. When clear leader is present at the start of a function, the transition onto opaque tape restarts the timer. The CTA changes from write to error mode if it senses clear leader for greater than 3.0 sec. or if data is not detected from the cassette for 2.8 sec. after receiving WRT function. The CTA erases tape in the forward direction when it receives a WRT function without data. The CTA changes from write to idle mode when it receives a STOP function.

READ MODE

The CTA is placed in the read mode if it is issued a read (RED) function code from the TCU. In this mode, stop/go (TGO.G/) is held Low; and write select (TWTSEL.G/), forward/reverse (TFWD.G), and slow/fast (TSLOW.G) are held High. The CTA holds TGO.G/ High for an additional 15 msec. if the previous operation performed by the CTA was backspace or erase operation. The BSY status is issued by the CTA until data is ready to be transferred to the TCU, at which time the status changes to RDY.

Read enable (TRDEN.G/) permits data from the transport 30 msec. after receiving a read (RED) function, until completion of the read operation. If clear leader is sensed when the read function is received, read enable inhibits data from the transport until 30 msec. after the BOT marker is detected.

The CTA contains a data timer which causes the CTA to change the status from BSY to EOM (end of message) if no data from the cassette is detected for 2.8 sec. after receiving a read function. When clear leader is present at the start of a read function, the transition onto opaque tape restarts the timer. If clear leader is sensed for greater than 3.0 sec., the CTA changes to the error mode; and the status is changed from BSY to ERR.

When data is detected in the CTA, the CTA performs several functions. The CTA strips the preamble, CRC, and postamble from the data. The data is prepared to be

adjusted to within ± 0.2 volts of the voltage listed on the reference amplitude cassette.

BOT-EOT

Test And Adjustment:
Connect the transport to the test box, power supply, or parent unit. Connect a scope probe to pin 5 of connector J1 on the read/write amplifier circuit board (bottom board). Load the BOT-EOT test cassette (603-9000850) into the transport with side B up. With the head pulled out and the semi-clear tape between the lamp and the sensor, adjust VR4 counterclockwise until the signal goes Low. Now, turn VR4 clockwise until the signal just goes High.

Turn the tape over to side A (dark side). Move the head in manually to verify that the tape cannot be recognized as leader. The signal on the scope should remain Low with the head held in manually.

NOTE: The BOT-EOT light transmittance test tape (603-9000850) is a short piece of tape fixed to the cassette case. Care should be taken not to energize the pinch rollers while using this tape. Side A is made of opaque tape which is a little more transparent than regular opaque recording tape. Side A is used when the recording head is pulled in; that is, the distance between the head and the hole sensor is at a minimum. The sensor should not be able to pick up light, so the signal at pin 5 of J1 should be Low. Side B is made of clear leader which is a little darker than the regular clear leader. When side B is used, the recording head is out at the maximum distance away from the sensor. The sensor should pick up the minimum amount of light from the lamp. The output at pin 5 of J1 should be High.

MICRO SWITCHES

Write Enable Switch SW3

Test And Adjustment:
Loosen the two screws holding the switch to the under side of the frame two full turns. Move the switch as far forward toward the magnetic head as the holes in the switch allow, and tighten both screws. Loosen the two screws holding the actuator spring to the under side of the main frame two turns. Move the spring until it barely contacts the plunger in its fully extended position, and tighten both screws with the spring in this position. Install an NCR-approved cassette with the write enable plug in place, and verify that the switch is fully actuated (plunger bottomed). If these conditions cannot be achieved, the actuator spring must be replaced or reformed.

Bend.

Cassette Side A Switch SW2

Test And Adjustment:
Loosen the two screws holding the switch two turns. Move the switch as far as possible to the rear away from the magnetic head assembly, and move the actuator spring as far forward as the mounting holes allow. Tighten the two screws holding the switch and actuator. Loosen the two screws holding the micro switch bracket to the head solenoid two turns. Insert an NCR-approved cassette side B up. Move the bracket forward until the switch plunger is bottomed, and tighten both screws. Remove the cassette and reinsert with side A up. Verify that the switch is not actuated. If these conditions cannot be achieved, the actuator spring must be replaced or reformed.

Bend.

Cassette Presence (SW1) and Capstan Motor Switch (SW4)

Test And Adjustment:
Loosen the two screws holding the switch two turns. Move the switch as far forward toward the magnetic head assembly as the holes allow. Tighten both screws with the switch in the forward position. Loosen the two screws holding the actuator spring to the under side of the main frame two turns. Move the actuator spring as far toward the switch as the mounting holes allow, and tighten the screws. Install an NCR-approved cassette, and verify that the switch is actuated (bottomed). Remove the cassette, and verify that the switch is deactivated (plunger fully extended). If these conditions cannot be met, the actuator spring must be replaced or reformed.

Bend.

If the BOT/EOT marker is detected while over a data field, the CTA issues BSY status instead of EOM following the detection of an IRG and changes to BET status instead of IDL 25 msec. after the stop command is issued.

The use of a stop function as an abort function requires special attention. The CTA aborts the erase operation and stops tape movement immediately after receiving a stop function. The tape can stop over the data field or an improper position in the IRG. The next operation can be in error because of improper position of the tape.

Forward erase can be performed by issuing a WRT function without sending data.

REWIND MODE

The CTA goes into the rewind mode when it has received a RWD function. If a RWD function is issued by the TCU when the CTA senses clear leader, the CTA goes into the error mode and issues an ERR status within the next character time.

When in the rewind mode, the CTA places BSY status on the bus and permits the cassette to rewind by causing stop/go (TGO.G/), forward/reverse (TFWD.G), and slow/fast (TSLOW.G) to go Low and write select (TWSEL.G/) and read enable (TRDEN.G/) to go High. If the previous operation performed by the CTA is read or write, the CTA delays stop/go (TGO.G/) from going Low for 15 msec.

When the following conditions occur, the CTA changes from rewind to idle mode.

1. The BOT/EOT marker is detected. It is possible that the transport may or may not detect a BOT/EOT marker while in the rewind mode.
2. The CTA receives a stop function.
3. Clear leader is sensed on the tape.

IDL status is sent to the TCU 255 msec. after the stop function is issued from the TCU.

POWER SUPPLY M32-1-761

INTRODUCTION

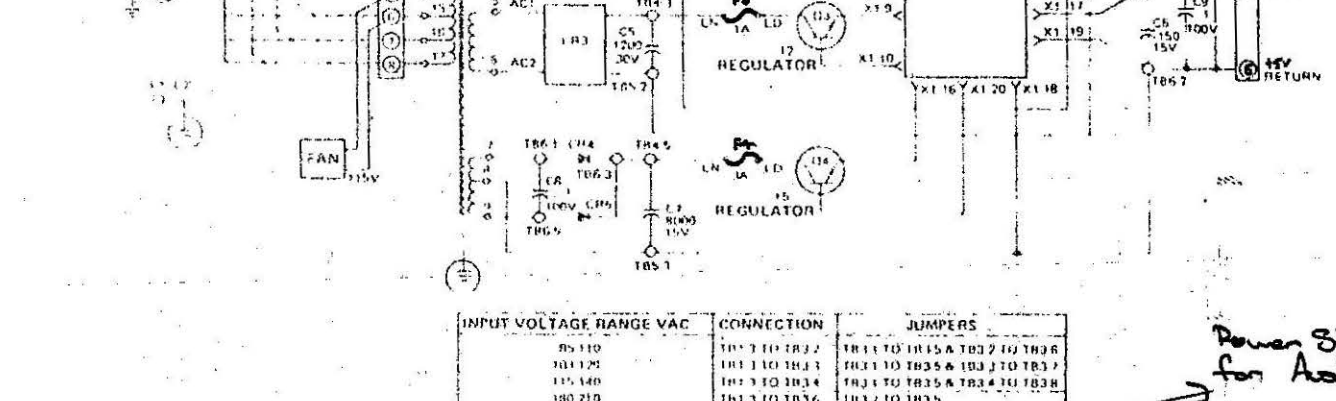
The M32-1-761 power supply is a compact modular unit which is incorporated in the NCR 761 Cassette Terminal Recorder to provide dc operating voltages for the Cassette Terminal Adapter module (M64-1-761) and the Cassette Transport module (M63-2-STD). The power supply produces three series regulated dc voltages (+12 vdc at 0.55 a., -12 vdc at 0.26 a., and +5 vdc at 2.0 a.) over a wide range of ac input voltages at either 50 or 60 Hz.

The regulating circuits for the dc output voltages are contained on a single circuit card. Additional circuitry on this card provides overvoltage protection for the +5 vdc output only. Current limiting protection (short circuit) for all three voltages is also a function of the regulating circuits.

PHYSICAL DESCRIPTION

The power supply module is located over the Cassette Terminal Adapter cards on the left side of the 761. The module is secured by three mounting screws and occupies an area 7.75 inches wide, 3.25 inches high, and 8.5 inches deep. The front plate contains all of the fuses used in the unit. Figure 27 illustrates the power supply circuitry.

Terminal board functions in the power supply are as follows. The ac input line and the power ON switch are



INPUT VOLTAGE RANGE VAC	CONNECTION	JUMPERS
85-110	TB1 1 TO TB3 2	TB3 1 TO TB3 5 & TB3 2 TO TB3 6
101-125	TB1 1 TO TB3 3	TB3 1 TO TB3 5 & TB3 3 TO TB3 7
115-140	TB1 1 TO TB3 4	TB3 1 TO TB3 5 & TB3 4 TO TB3 8
180-210	TB1 1 TO TB3 6	TB3 2 TO TB3 5
201-240	TB1 1 TO TB3 7	TB3 2 TO TB3 5
220-250	TB1 1 TO TB3 8	TB3 3 TO TB3 5

Power Strapping for Australia

Fig. 27 Power supply schematic

connected to TB1. The dc voltage outputs are connected to TB2. The primary winding of transformer T1 is strapped at TB3 to accommodate the various ac input voltages that may be encountered. Terminal boards TB4, TB5, and TB6 are used internally by the power supply for component interconnection.

The heat sink contains the pass transistors and the driver transistors for the +12 v., -12 v., and the +5 v. supplies. Located on the chassis, directly behind the heat sink, are the power transformer T1, rectifiers CR1 through CR5, and miscellaneous filter capacitors C1 through C9.

The power supply uses a single circuit card for all regulating and circuit protection functions. The functions of the major components are as follows. The hybrid circuit packs U1, U2, and U3 which are the regulating circuits for the +5 volts, -12 volts, and the +12 volts, respectively. Transistors Q2 (+5 volts) and Q3 (-12 volts), function as pass section drivers for the voltages specified. Overvoltage protection for the +5 volts is provided through the use of transistor Q1 and silicon controlled rectifier SCR1.

FUNCTIONAL DESCRIPTION

The power supply is divided into five segments. These segments are the power supply input, the bias supply, the +12 vdc supply, the -12 vdc supply, and the +5 vdc supply.

The ac input is applied to the primary of power transformer T1 through TB3. The strapping of the power supply is between TB-1 and TB-3 to accommodate the various ac line voltages. Domestically, the unit is strapped to accept 115 vac at 60 Hz.

The output of transformer T1 supplies power to the bias supply and each of the dc output voltage supplies. The bias supply provides a dc voltage used to operate the +12 v. regulator circuitry. The +12 vdc output is then routed to the remaining circuits and used as a regulating voltage.

The three dc supply networks operate in the same manner. The ac input voltage is rectified and filtered into an unregulated dc voltage which is routed to the pass section. The pass section in conjunction with the regulator circuit, regulates the dc voltage to the correct level.

The regulator circuit continually samples the power supply output for any variations. Any change in the output causes the regulator circuit to transmit a correction signal to the pass section which electronically adjusts the output back to normal. Each supply network in the power supply is designed to produce the desired voltage with no external adjustments being required.

The +5 vdc supply network contains an overvoltage protection circuit which short-circuits the output in the event of an overvoltage condition. This causes the +5 vdc supply to enter a current limit condition which shuts the supply down and prevents any circuit damage. Since the TTL logic is extremely sensitive to overvoltage conditions this circuit is necessary. The TTL logic uses the +5 vdc almost exclusively.

Each segment of the power supply is explained in detail with the exception of the regulator card. Description of the regulator card is more general in nature due to the card exchange philosophy dominate with NCR terminal equipment.

POWER SUPPLY INPUT

The power supply input segment comprises terminal boards TB1 and TB3, fuse F1, and the primary of power transformer T1. As shown, the ac line cord is connected to TB1-1. The ac ground wire from the line cord is connected

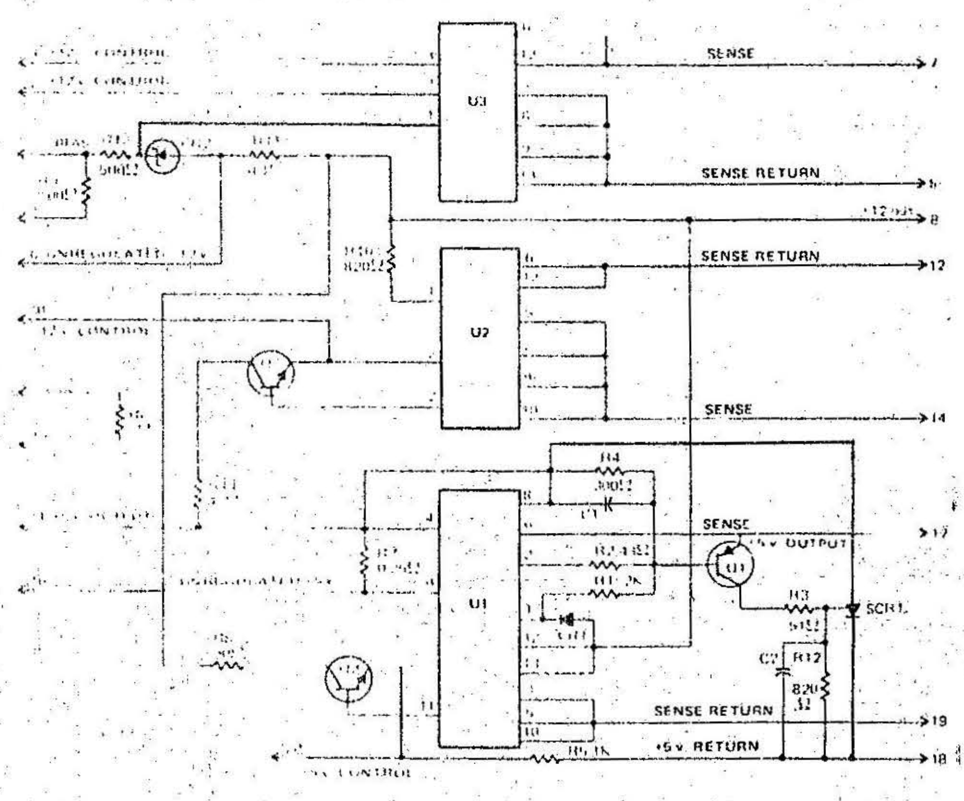


Fig. 28 Regulator circuit card schematic

to the chassis ground lug E1. The POWER ON switch is connected between terminals TB1-1 and TB1-2.

Strapping T1 for the correct ac input voltage is explained later in this section. For domestic purposes, the unit is strapped in the 103-127 vac range. Input frequency is not a consideration because the transformer is capable of operating at 50 Hz or 60 Hz.

When the POWER ON switch is placed in the ON position, ac current flows from the wall plug to TB1-1, through the switch to TB1-2, through fuse F1 to TB3-1 and the primary of transformer T1. The ac return path from the primary of T1 is from TB3 through TB1-N back to the wall plug.

Fuse F1 protects the input circuit against excessive current through the transformer.

BIAS SUPPLY

The bias supply generates a unregulated +10.5 vdc which is used as the operating voltage for the +12 vdc regulator circuit. The bias supply comprises the full-wave bridge rectifier CR1 and the filter capacitor C1.

The positive dc output of the supply is routed to the +12 vdc regulator circuit through card connector X1-3. The reference side of the supply is connected to the unregulated portion of the +12 vdc supply at the collector of pass transistor Q1. Since the bias supply is not referenced to chassis ground, voltage measurements must be made across capacitor C1 to receive a true reading.

+12 VDC SUPPLY

The +12 vdc supply is a regulated supply comprising the full wave bridge rectifier CR2, filter capacitor C3, fuse F2, pass transistor Q1, pass driver transistor Q2, the +12 vdc regulator circuit (located on the regular circuit board), and the output filter capacitor C2. The regulator circuit has built in short-circuit protection which shuts the supply down if a short occurs across the output terminals. No overvoltage protection is provided.

The circuit operation is as follows. The secondary ac voltage felt at pins 3 and 4 of transformer T1 is rectified by CR2 and C3 and filtered into an unregulated +17.5 vdc. The negative side of C3 is the +12 vdc common and is connected directly to the supply output at TB2-3 (+12 v. RETURN).

The unregulated +17.5 vdc is routed through protective fuse F2 to the collector of pass transistor Q1. The degree of conduction of Q1, which is controlled by pass driver transistor Q2, determines the output voltage of the supply at TB2-1. Transistor Q2 is controlled by the +12 vdc regulator circuit which receives its operating power from the bias supply at connector X1-3.

The regulated +12 vdc output from the regulator board is routed from the card connector X1-8 to TB2-1. Capacitor C2 provides final filtering for the output voltage. The lines that are connected from card connector X1-7 and X1-5 across the dc output are the sense lines to the +12 vdc regulator circuit.

The sense lines are used by the regulator circuit to detect changes in the output voltage. An increase in the rated output causes the regulator circuit to send a negative going error signal through card connector X1-2 to the base of Q2. This decreases the conduction of Q2 and, in turn, causes a decrease in the conduction of Q1. Accordingly, Q1 allows less of the unregulated +17.5 vdc to be felt at the output of the supply. A decrease in the rated output voltage causes an opposite reaction by the regulating circuitry.

The regulated +12 vdc is routed internally on the regulator circuit card to provide operating power for the -12 vdc and +5 vdc regulating circuits.

-12 VDC SUPPLY

The -12 vdc supply is a regulated supply comprised of full wave bridge rectifier CR3, filter capacitor C5, protective fuse F3, pass transistor Q3, the -12 vdc regulating circuitry (located on the regulator circuit board), and the output filter capacitor C4. The regulator circuit provides short-circuit protection which shuts the supply down if a short occurs across the output terminals.

The circuit operation is identical to the +12 vdc supply in that the regulation of the supply voltage is performed in the positive leg of the output. Rectifier CR3 and filter capacitor C5 produce an unregulated +17.5 vdc which is routed through fuse F3 to the collector of pass transistor Q3.

The degree of conduction of Q3, and consequently the output voltage, is controlled by the regulating circuitry on the regulator circuit card. However, since the positive output of the regulator circuit is connected to the common reference line at TB2-4 (-12 v. RETURN), the negative leg of the supply at TB2-2 appears to be a -12 vdc in respect to the return line.

Controlling the positive leg of the supply in order to regulate the negative leg is possible because the -12 vdc supply has no internal chassis grounds.

+5 VDC SUPPLY

The +5 vdc supply is a regulated supply comprised of full wave rectifier CR4 and CR5, filter capacitor C7, protective fuse F4, the +5 vdc regulating circuitry (located on the regulator circuit card), and output filter capacitors C6 and C9. The regulator has built-in short-circuit and overvoltage protection which shuts the supply down in the event either condition occurs. Capacitor C8, across the secondary pins 7 and 9 of transformer, T1 is used as a noise filter.

Operation of the +5 vdc supply is the same as the +12 vdc supply in principle. The full wave rectifier and filter capacitor C7 produce an unregulated +9 vdc. This voltage is routed through fuse F4 to the collector of pass transistor Q4. The degree of conduction of Q4 determines the voltage felt at the output of the supply, and the +5 v. regulator controls the conduction of Q4 through card connnector X1-20.

The positive regulated output of the +5 v. regulator at card connector X1-11 is routed to the supply output at TB2-6. This output is constantly sampled by the regulator at card connector X1-17. Any deviation in the output voltage causes the regulator to change the base voltage of Q4 and adjust the output back to normal.

The +5 v. supply has an overvoltage protection circuit

located on the regulator circuit board and connects directly across the supply output which activates at voltages between +5.5 v. and +6.5 v. When active, the overvoltage protection circuit shorts out the supply output and causes the regulator to go into a current limit condition. In effect, the supply shuts down as it would in a short-circuit condition.

Once activated, the overvoltage protection circuit does not restore until the condition causing the fault is corrected and ac power is removed and restored to the unit. A complete circuit description of the overvoltage protection circuit is presented in the Regulator Circuit Card Operation description.

REGULATOR CIRCUIT CARD OPERATION

The circuit schematic of the regulator circuit card is shown in figure 28. This description is general in nature since field repairs are made on a card exchange basis.

The regulator circuits are hybrid packs and are illustrated in block form on the schematic. Discrete transistor components Q2 and Q3 are pass driver transistors for the +5 vdc and -12 vdc respectively.

Transistor Q1, silicon controlled rectifier SCR1, and miscellaneous components makeup the +5 vdc overvoltage protection circuit. As shown, SCR1 is connected directly between the +5 vdc output and the +5 vdc return.

The emitter of Q1 is connected directly to the +5 vdc output, and the base is connected to a voltage divider network (R1, R2, and R4). The base voltage of transistor Q1 is regulated at +5 vdc by the action of a zener diode in hybrid pack U1. As long as the output voltage remains at a normal level, the base to emitter difference of potential biases Q1 OFF.

An increase in the output voltage to +5.5 v. causes the base to emitter difference of potential to bias Q1 ON. With Q1 ON, current flows from the +5 v. output line through Q1, R3, and R12 to the +5 v RETURN. A positive voltage drop is felt across R12 to the gate of SCR1 causing SCR1 to turn ON and short the +5 vdc output line to the return line. This causes the +5 vdc regulator to go into a current limit condition and effectively shut the supply down.

Once SCR1 has turned ON, it cannot be turned OFF unless ac power is removed from the unit.

SERVICE INFORMATION

TEST AND ADJUSTMENT

The only adjustment to the M64-1-761 is the clock adjustment on the TTL circuit board. This adjustment provides the correct timing to block out the insignificant transitions of the cassette tape signal. Before this adjustment can be made it is necessary that the speed of the transport be accurate. Use a test tape with a continuous 0101010101010101010101 data format. Connect probe number 1 of a dual trace oscilloscope to TP-3 (red) and trigger internal positive. Connect probe number 2 to TP-4 (orange). Ground for the scope can be found at TP-1 (black). The scope pattern should appear as in figure 29. Position the service switches for test mode, forward, and go. If TX is not equal to 110 µsec., adjust potentiometer R42 for the correct value.

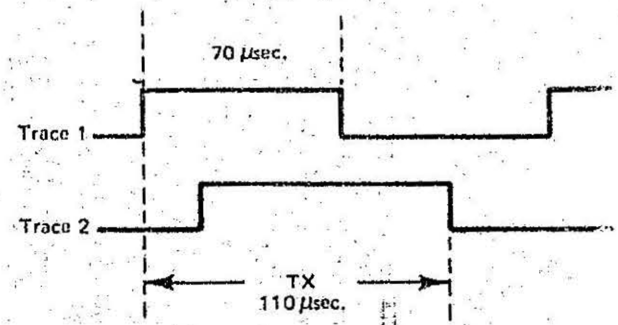


Fig. 29 Clock adjustment

PREVENTIVE MAINTENANCE

The 761 cassette terminal recorder consists of the following modules. The maintenance required for each module is listed below.

1. M24-1-STD Remote cable; requires no preventive maintenance.
2. M30-1-761 Miscellaneous module; requires no preventive maintenance.
3. M32-1-761 Power supply module; requires no preventive maintenance.
4. M63-2-STD Transport module; requires preventive maintenance as described in MS-413, Cassette Transport Field Service and Training Manual.
5. M64-1-761 Cassette Terminal Adapter module; requires no preventive maintenance.